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**H-316-20 DATA MULTIPLEX  
MULTIPLEX CONTROL OPTION**

Order No. 70130072180L   Order No. FT13

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## **H-316-20 DATA MULTIPLEX MULTIPLEX CONTROL OPTION**

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June 1975

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## H316-20 DATA MULTIPLEX CONTROL

### INTRODUCTION

The data multiplex control (DMC) option provides direct access for input/output data transfers between the memory of the H316 General Purpose Digital Computer and external devices requiring this service.

Multiplexed service provides either 4, 8, 12, or 16 channels, each being serviced according to its priority. Channel 1 has the highest priority and channel 16 the lowest.

The H316-20 option requires four 1.6  $\mu$ sec cycles for each data transfer.

#### Reference Documents

<u>Title</u>	<u>Doc. No.</u>
H316 Central Processor Description	70130072176
H316 Central Processor Instructions and Logic Diagrams	70130072174
H316 Interface Manual	70130072167

#### Physical Characteristics

The DMC option consists of integrated circuit  $\mu$ -PACs packaged in a 2 x 3 BLOC. This BLOC is inserted into the H316 main frame drawer.

#### Functional Description

The DMC is a passive device that responds to the needs of the devices which use its control lines. (See Figure 1.) When a particular device has data to input, or is ready to accept data, the device then uses the DMC control lines to request service. The DMC will then send a break request to the CPU. A DMC cycle will be executed when the current instruction has been completed; however, in the case of a multiple cycle instruction, such as a shift, the break request will be honored before the instruction is completed. During this cycle the appropriate transfer between the device and the memory will take place, using the standard I/O bus.

### OPERATION

Instructions for operating the various DMC devices can be found in operation instructions for that particular unit. Preliminary programming necessary for operating a device is:

- a. Store the starting address, with bit 1 a ONE for input mode, ZERO for output mode, in the assigned location for the starting address. (See Table 1.)

- b. Store the ending address in assigned location for ending address. (See Table 1.)
- c. Using appropriate OCPs, set up the device in the input or output mode and set up the DMC mode. The order of these OCPs is specified in each device specification.
- d. If a program interrupt is to be used to detect end of data transmission, the PI mask flip-flop for the device must be set up to a ONE, and the desired interrupt routine must be part of the program.

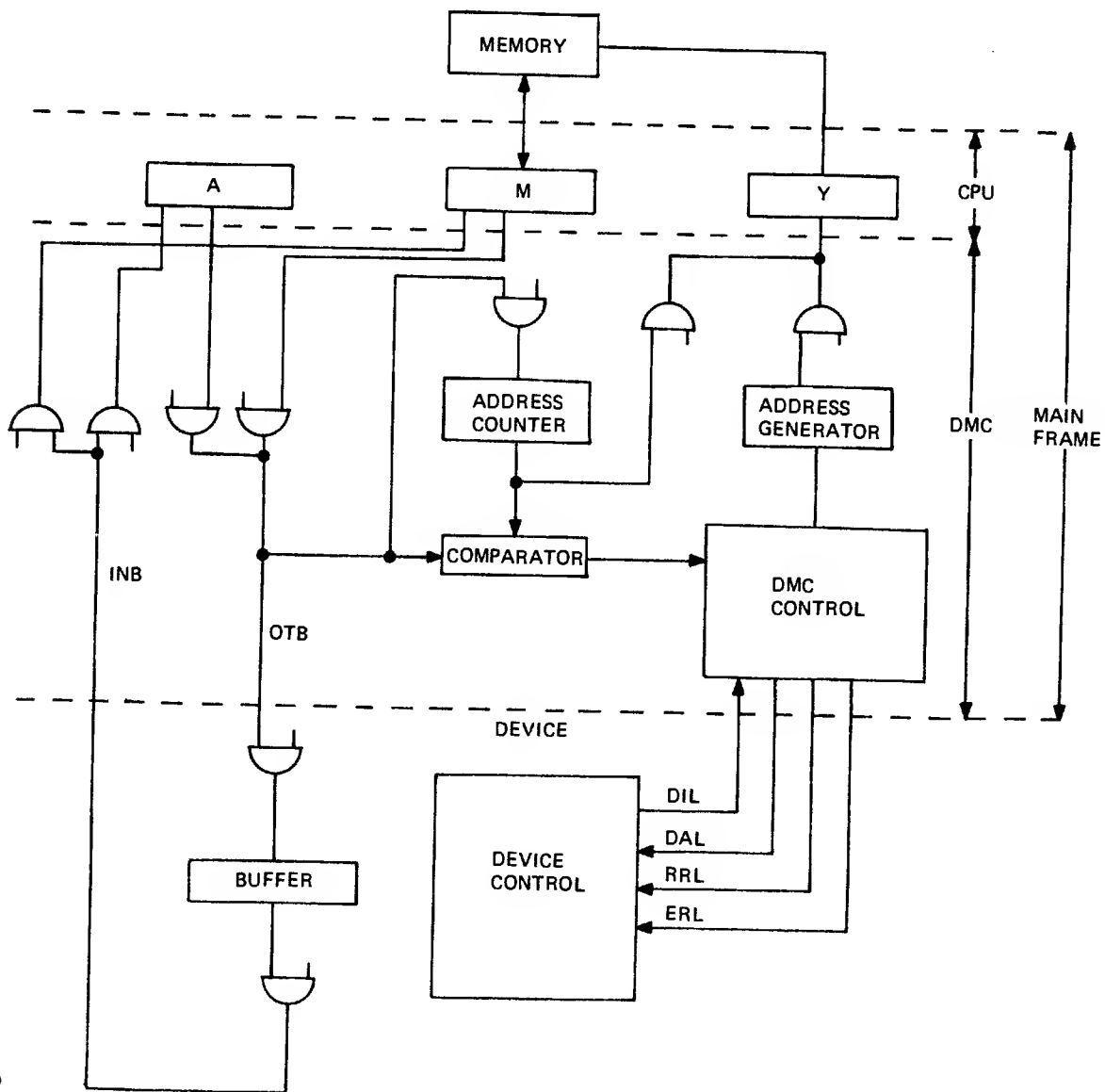


Figure 1. DMC Signal Interface Block Diagram

Table 1.  
Starting and Ending Address Locations

<u>Channel No.</u>	<u>Starting Address</u>	<u>Ending Address</u>
1	00020	00021
2	00022	00023
3	00024	00025
4	00026	00027
5	00030	00031
6	00032	00033
7	00034	00035
8	00036	00037
9	00040	00041
10	00042	00043
11	00044	00045
12	00046	00047
13	00050	00051
14	00052	00053
15	00054	00055
16	00056	00057

## INSTALLATION

### PAC Locations

The DMC option consists of integrated circuit  $\mu$ -PACs packaged in a 2 x 3 BLOC. This BLOC is inserted into the H316 main frame. (See PAC allocation drawing, LBD No. 239.)

### Power Source

The DMC unit power requirements are supplied by the main frame power supply.

### Interface Connections

Connections between the I/O bus and interface logic for the DMC are shown on LBD No. 238. For further information, refer to the H316 Interface Manual, Doc. No. 70130072167.

## THEORY OF OPERATION

Refer to Table 2 for a list and descriptions of DMC mnemonics. See Figure 1, a block diagram of the DMC signal interface, and LBD No. 231 through LBD No. 238 for DMC logic.

### NOTE

Starting with Revision E, all H316 HSDMC options will be able to break during an F, I, or A cycle except during the first A cycle of a three-cycle instruction (JST, IRS, etc.) or the F cycle of an I/O instruction. Therefore, the maximum latency for any instruction is two cycles.

Table 2.  
Function Index

<u>Mnemonic</u>	<u>Description</u>
ADREN	Address enable to IY bus
CLDCR	Clear address counter
CLEAR	Clear priority network
CLMTR	Clear M-register storage
CO112	Carry out from any of channels 1 through 12
CO14X	Carry out from any of channels 1 through 4
CO116	Carry out from any of channels 1 through 16
CO18X	Carry out from any of channels 1 through 8
DALEN	Device address line enable
DALnn	Device address line, channels 1-16
DCRnn	Address counter register bit nn
DCY2X	DMC cycle, phase 2
DCY3X	DMC cycle, phase 3
DILnn	Data interrupt line, channels 1-16
DMC1X	DMC cycle, phases 1 and 2
DMC2X	DMC cycle, phases 2 and 3
DMCCY	DMC cycle
DMCRQ	DMC request
DMCWR	DMC write/read level to memory
DMCYQ	DMC cycle (CPU)
DRQnn	DMC request, channel nn
DMRRL	DMC reset ready line
EAMTS	Emit address to M-register timing strobe
EENBL	Enable timing level E
EMMTA	Emit M-register storage to CPU M-register
EOIDR	End of instruction and DMC request
EORTS	Output bus to address counter (gating signal)
ERLXX	End of range
EIMTS	Emit input bus to M-register strobe
EMDTS	Emit CPU M-register to M-register storage
INBnn	Input bus, bits 1-16
INRT2	Inhibit repeat TL2
IYBnn	Input to Y-register bus, bits 2 through 16 used by DMC option and program interrupt
MnnDF	M-register storage
MADCL	Memory address clear
MCSET	Master clock, set phase
MSTCL	Master clear (overall initialization)



Table 2. (Cont)  
Function Index

<u>Mnemonic</u>	<u>Description</u>
OBINH	CPU output bus inhibit
OTBnn	Output bus, bits 1-16
RRLIN	Reset ready line
SAMPL	Sample DILs
SETTA	Set TLAFF signal
SETTB	Set TLBFF signal
SETTC	Set TLCFF signal
SETTD	Set TLDFF signal
SETTE	Set TLEFF signal
SETTF	Set TLFFF signal
TACFF	Timing level A through timing level C flip-flops
TBDFF	Timing level B through timing level D flip-flops
TEFFF	Timing level E through timing level F flip-flops
TL1FF	Timing level TL1
TL2FF	Timing level TL2
TL3FF	Timing level TL3
TL4FF	Timing level TL4

#### Timing Level Generator

The DMC timing level generator (LBD No. 232) generates the various timing levels required for a DMC cycle. A DMC request (DMCYQ) enables the CPU master clock oscillator outputs MCSET, MCRST, and MTLG, to trigger the DMC timing level flip-flops. There are six of these flip-flops: TLAFF, TLBFF, TLCFF, TLDFF, TLEFF, and TLFFF. The transition from one level to the next is controlled by TACFF, TBCFF, TEFFF, and EENBL. Note that the TL4FF flip-flop (LBD No. 118) is inhibited while the DMC timing level generator is enabled.

During DMC cycles, timing levels TLA and TLE, followed by TLB and TLF occur simultaneously except at the beginning of the first cycle, when only TLA followed by TLB is generated, and the end of the last cycle, when only TLE followed by TLF is generated. The levels for one DMC transfer are generated as shown below. If successive transfers follow, then timing levels E and F are overlapped with A and B and timing level 4 does not occur until DMC requests are not pending.

	Start DMC																End DMC			
Timing Levels	3	A	B	C	D	E/A	F/B	C	D	E/A	F/B	C	D	E/A	F/B	C	D	E	F	4

Each channel has one DILXX line and one DALXX line. A device uses one of the DILXX lines to request a DMC cycle when it has data to input or is ready to accept data. The DMC will then send a break request to the CPU. A DMC cycle will be executed when the current instruction has been completed; however, in the case of a multiple cycle instruction, such as a shift, the break request will be honored before the instruction is completed.

The DALXX lines are used to notify a device that its request has been honored and a DMC cycle is currently being executed.

The DMC executes an input if bit 1 of the starting address location is a ONE. An output is executed if bit 1 is a ZERO.

Bits 2 through 16 of the starting address specify a memory location where the data on the input bus will be stored when a DMC input is executed. The data in this location will be transferred to the device via the output bus when a DMC output is executed.

RRLIN is generated during each DMC cycle to notify the device that the data transfer is complete.

If the device is in the input mode, it uses DALXX to gate its data onto the input bus. If the device is in the output mode, it uses the coincidence of DALXX and RRLIN to strobe the data on the output bus into its buffer. Note that when in the output mode, the device must not gate data onto its input bus.

During each DMC cycle, the contents of the starting address location will be increased by one. The first of the DMC transfers concerns the memory location initially stored in the starting address location. The second transfer concerns the next higher memory location, etc.

The terminal address is compared with the starting address during each DMC cycle. An end-of-range (ERLXX) signal is generated upon equality. The device may gate DALXX with ERLXX to inhibit further generation of requests. It may also generate an interrupt upon receipt of ERLXX.

### Synchronization

Sync cycles occur when the DMC is not executing a DMC cycle. During this sync cycle, the DIL lines are interrogated. If a DIL is detected, a computer break is requested. The DMC will then send a break request to the CPU. A DMC cycle will be executed when the current instruction has been completed; however, in the case of a multiple cycle instruction, such as a shift, the break request will be honored before the instruction is completed.

### DMC Cycle

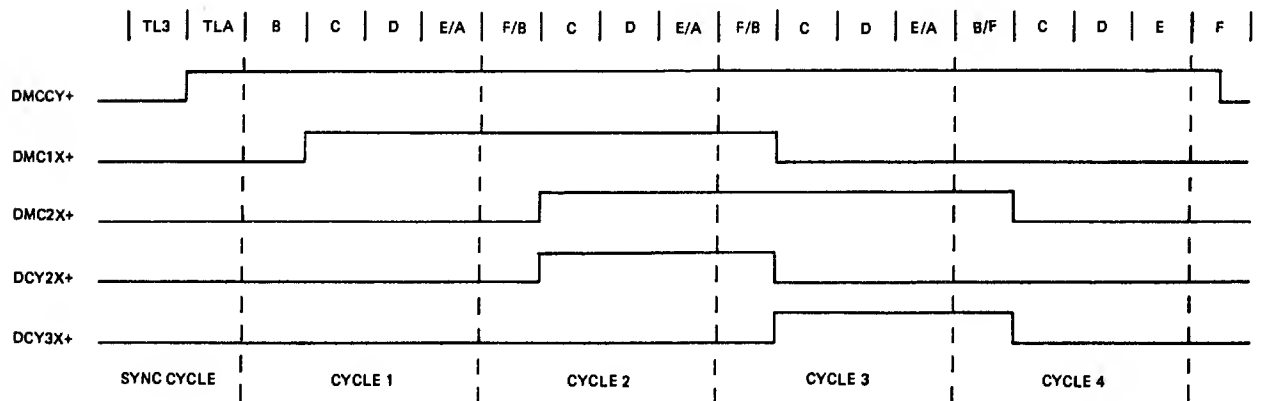
The standard DMC (H316-20) requires four 1.6  $\mu$ s cycles for each data transfer.

The DMCWR flip-flop controls the direction of the four DMC memory cycles. When it is set, a write cycle is executed. When reset, a read cycle is executed.

The sequence of the DMC operations is controlled by the DMC master clock (LBD No. 232) and the DMC1X and DMC2X flip-flops (LBD No. 232). They are used to generate the memory cycles shown in Figure 2.

The purpose of each memory cycle is as follows:

- a. Fetch Starting Address. -- The contents of the starting address location are fetched and stored in the address counter register.
- b. Fetch Terminal Address. -- The contents of the terminal address location are fetched and compared with the contents of the address counter register.
- c. Data Transfer. -- The data transfer is controlled by the contents of the address counter register. If bit 1 is a ONE, an input is executed. If bit 1 is a ZERO, an output is executed. The contents of the address counter are increased by one.
- d. Store Updated Starting Address. -- The contents of the address counter register are stored in the starting address location. If another DMC request is waiting, another DMC cycle starts. If no requests are waiting, the CPU resumes control.



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Figure 2. DMC Cycles

## DETAILED ANALYSIS

### Sync Cycle

The priority network is cleared by  $TL2FF \cdot MCRST$  of every sync cycle (CLEAR).  $SAMPL$  is generated by every  $TL2FF \cdot MCSET$ . If any  $DIL$  is true during  $SAMPL$ , the corresponding channel flip-flop in the priority network is set. (See Figure 3.) (Refer to Appendix A for the flow chart and analysis.)

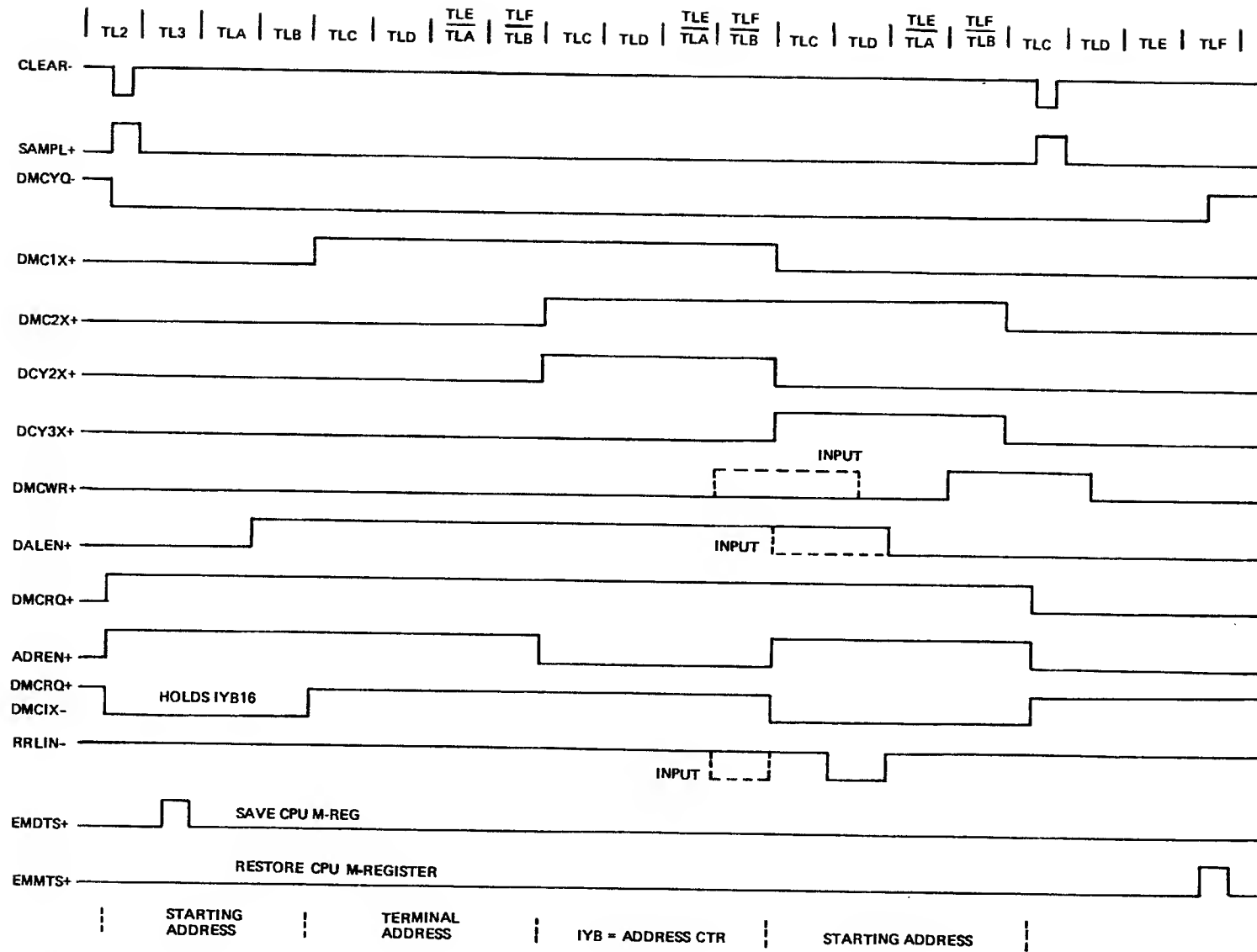


Figure 3. DMC Timing Cycle

The data in the M-register of the CPU is saved in the DMC every  $TL3 \cdot MCSET$ , and cleared every  $TL2 \cdot MCRST$ . Therefore, the contents of the CPU M-register are saved throughout the DMC break.

When any of the channel flip-flops are set, the priority network (PN) notifies the CPU that a device has requested a DMC cycle by generating DMCYQ. DMCYQ prepares the CPU for the execution of the DMC cycle by doing the following:

- a. Inhibiting all the transfer paths to the Y-register other than the IY bus.
- b. Inhibiting PIL00 and SEX from using the IY bus.
- c. Inhibiting CPU timing level generator at the end of TL3.
- d. Inhibit RPTT2.
- e. Saving NRMOP.
- f. Inhibiting IOACY.

These steps allow the CPU to complete the current instruction but prevent the starting of another instruction.

The priority network operates in a manner such that the highest priority channel flip-flop, of those which are set, enables the starting address location for that channel to appear on the IY bus. For example, if channel flip-flops 2, 7, and 9 are set,  $(000022)_8$  will appear on the IY bus. SAMPL and CLEAR are inhibited until the end of the DMC cycle so that, after having decided on priority and started the DMC cycle, the output of the priority network remains fixed.

EOINS is a level generated by the CPU which becomes true during the last cycle of each computer instruction. When DMCQR and MPY, DIV or EOINS occur, the first DMC cycle is initiated.

At TLAFF time, the IY bus is strobed into the Y-register. The DMCWR flip-flop is in the reset state.

#### First DMC Cycle

At TLBFF time MEMCI occurs. This set of conditions produces a memory cycle which fetches the contents of the starting address location and stores them in the M-register. (Refer to Appendix A for the flow chart and analysis.)

During the DMC cycle, the contents of the M-register are gated to the output bus (LBD No. 238).

EORTS+ (LBD No. 236) is used to strobe the contents of the output bus into the address counter register. This completes the fetch of the starting address.

The priority network continues to apply the starting address location to the IY bus. The terminal address location is always an odd number and one higher than the starting address (Table 1); therefore, bit 16 of the IY bus is changed from a ZERO to a ONE. This produces the terminal address location on the IY bus which is strobed into the Y-register at TLAFF time.

### Second DMC Cycle

Because DMCWR+ is still reset, the resulting memory cycle fetches the contents of the terminal address location which subsequently appears on the output bus. This address is compared with the starting address which is currently in the address counter. (Refer to Appendix A for the flow chart and analysis.)

The comparator (LBD 237) is a 15-bit exclusive OR network. The output is true if the 15 low order bits of the output bus are equal to the 15 low order bits of the address counter register, respectively.

ERLXX- is generated if the output of the comparator is true.

The 15 low order bits of the address counter register will be transferred to the Y-register via the IY bus to provide the memory address of the third DMC cycle, which performs the data transfer.

### Third DMC Cycle

If bit 1 of the address counter register is set, an input transfer is called for, and the following operations are carried out:

- a. DMRRL (LBD 238) is sent to the CPU to generate RRLIN (LBD 232) indicating that the data on the input bus has been taken.
- b. The contents of the input bus are strobed into the M-register at TLB.
- c. The DMCWR flip-flop is set so that the following memory cycle writes the contents of the M-register into the memory.
- d. The DALEN flip-flop is reset, disabling all DAL lines and also clearing the input bus for use by the DMC.

If bit 1 of the address counter register is reset, an output transfer is called for and the following operations are carried out:

- a. In the output mode the contents of the memory location, specified by the 15 low order bits of the address counter register, appear on the output bus after TLC. RRLIN- (LBD 232) is generated by DMRRL (LBD 238).
- b. The device ANDs DALnn with RRLIN to strobe the contents of the output bus into its buffer. (Refer to the Appendix for the flow chart and analysis.)
- c. The DALEN flip-flop is reset, disabling all DAL lines.

For either input or output, the starting address is updated. The count pulse generated adds one to the contents of the address counter register.

### Fourth DMC Cycle

The contents of the address counter register are then gated into the M-register. The DMCWR flip-flop is set so that this address is stored during the fourth DMC cycle.

The contents of the M-register are transferred to memory to complete the operations necessary for updating the starting address. (Refer to Appendix A for the flow chart and analysis.)

SAMPL is generated, permitting the priority network to be cleared by the CLEAR pulse (LBD 233). TLC generates SAMPL. If any of the channel flip-flops are now set, DMCYQ is sent to the CPU, requesting another DMC cycle. EOIMD is true during the fourth memory cycle of the DMC cycle; therefore, another DMC cycle can immediately follow. DMC cycles continue until all DIL lines are reset.

If no DIL lines are set, the contents of the DMC M-register are transferred to the CPU M-register.

If the CPU has completed its current instruction prior to the DMC break, MEMCI initiates the fetch of the next instruction. If the CPU has not completed its current instruction prior to the DMC break, the current instruction resumes.

#### Special Wiring

All unused channels must be wired as shown in the following wire chart.

<u>Channel</u>	<u>From</u>	<u>To</u>
1	A2103	A2113
2	A2105	A2123
3	A2110	A2111
4	A2116	A2130
5	A2203	A2213
6	A2205	A2223
7	A2210	A2211
8	A2216	A2230
9	A2303	A2313
10	A2305	A2323
11	A2310	A2311
12	A2316	A2330
13	A2403	A2413
14	A2405	A2423
15	A2410	A2411
16	A2416	A2430

#### PARTS LIST

This section supplements Chapter III of the H316 Circuit Modules and Parts Instruction Manual by including a parts complement of the Standard Data Multiplex Control option. The reference designation coding is in accordance with CCD coding Drawing 70023412, sheet 3 of 6, in the H316 Circuit Modules and Parts Instruction Manual. (See Figure 4.)

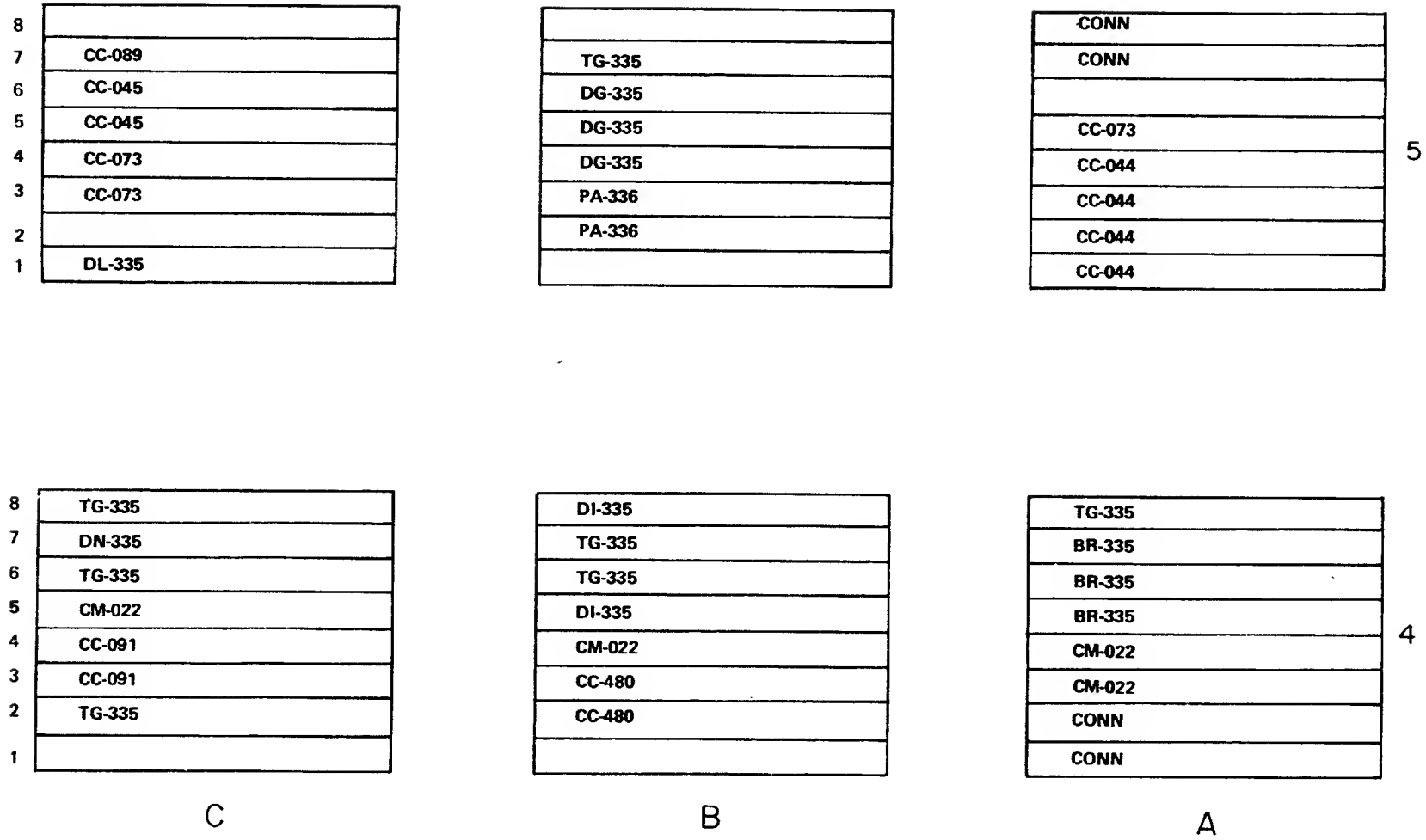


Figure 4. H316-20 Standard DMC PAC Layout



Fig. & Index No.	Designation	CCD Part No.	Description	Qty. per Assy.
4-	Located in the Logic Bay (A1)	70025573	STANDARD DATA MULTIPLEX CONTROL OPTION	1
	A1A405, A1A406, A1A407	BR-335	BUFFER REGISTER PAC (Refer to $\mu$ -PAC Instruction Manual, Vol. I, Section 2, Doc. No. 130071369, for parts break- down.)	3
	A1A501, A1A502, * A1A503, ** A1A504***	CC-044	PRIORITY PAC (Refer to Appendix B for parts break- down.)	A/R
	A1C505, A1C506	CC-045	NAND TYPE 1 POWER AMPLIFIER PAC (Refer to Appendix B for parts break- down.)	2
	A1A505, A1C503, A1C504	CC-073	NAND TYPE 2 POWER AMPLIFIER PAC (Refer to Appendix B for parts break- down.)	3
	A1C507	CC-089	GATED FLIP-FLOP PAC (Refer to Appendix B for parts breakdown.)	1
	A1C403, A1C404	CC-091	FAST CARRY COUNTER PAC (Refer to Appendix B for parts breakdown.)	2
	A1B402, A1B403	CC-480	DRIVER PAC (Refer to Appen- dix B for parts breakdown.)	2
	A1A403, A1A404, A1B404, A1C405	CM-022	PARALLEL TRANSFER GATE PAC (Refer to Appendix B for parts breakdown.)	4
	A1B405, A1B408	DI-335	NAND TYPE 1 PAC (Refer to $\mu$ -PAC Instruction Manual, Vol. I, Section 3, Doc. No. 130071369, for parts break- down.)	2
	A1B504, A1B505, A1B506	DG-335	SELECTION GATE TYPE 1 PAC (Refer to $\mu$ -PAC Instruc- tion Manual, Vol. I, Section 3, Doc. No. 130071369, for parts breakdown.)	3
	A1C501	DL-335	NAND TYPE 2 PAC (Refer to $\mu$ -PAC Instruction Manual, Vol. I, Section 4, Document No. 130071369, for parts breakdown.)	1
	A1C407	DN-335	EXPANDABLE NAND GATE PAC (Refer to the $\mu$ -PAC Instruction Manual, Vol. I, Section 4, Doc. No. 130071369, for parts breakdown.)	1

\*Added for 5-8 channels.

\*\*Added for 9-12 channels.

\*\*\*Added for more than 12 channels.

Fig. & Index No.	Designation	CCD Part No.	Description	Qty. per Assy.
	A1B502, A1B503	PA-336	POWER INVERTER PAC (Refer to $\mu$ -PAC Instruction Manual, Vol. I, Section 6, Doc. No. 130071369, for parts breakdown.)	2
	A1A408, A1B406, A1B407, A1B507, A1C402, A1C406, A1C408	TG-335	TRANSFER GATE PAC (Refer to $\mu$ -PAC Instruction Manual, Vol. I, Section 8, Doc. No. 130071369, for parts breakdown.)	7
	A1A401, A1A402	014998702	CABLE ASSEMBLY (Refer to Figure 5 for parts breakdown.)	2
	A1A507, A1A508	013826701	CABLE ASSEMBLY (Refer to Chapter III, Figure 3-13, Doc. No. 70130072166 for parts breakdown.)	2

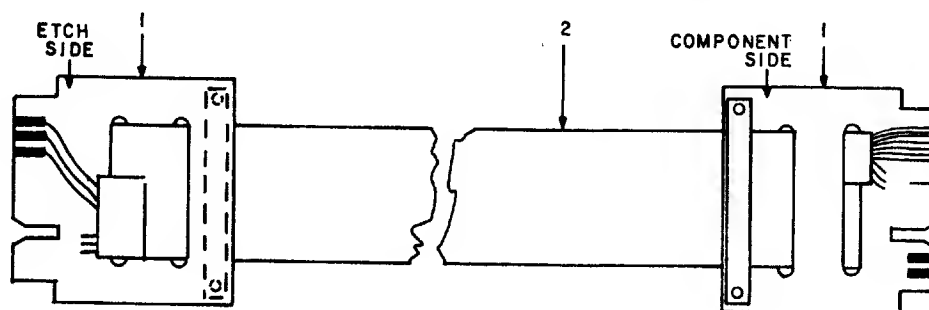


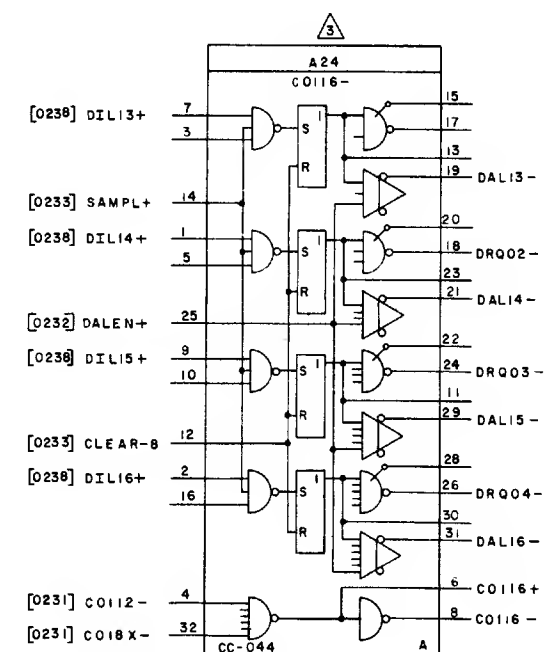
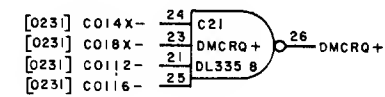
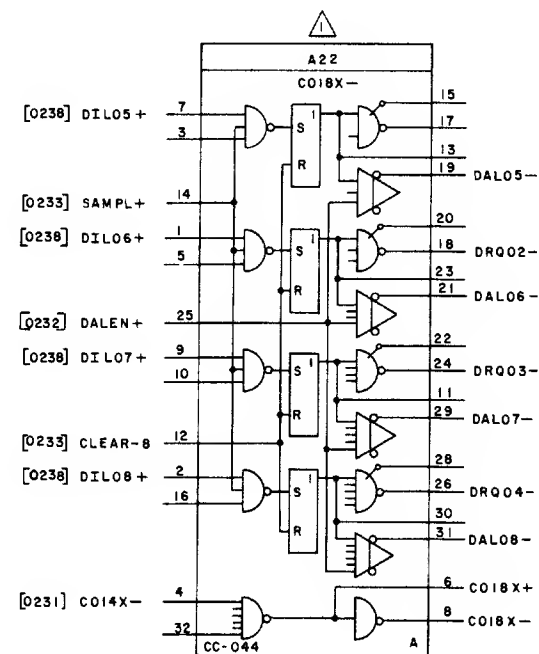
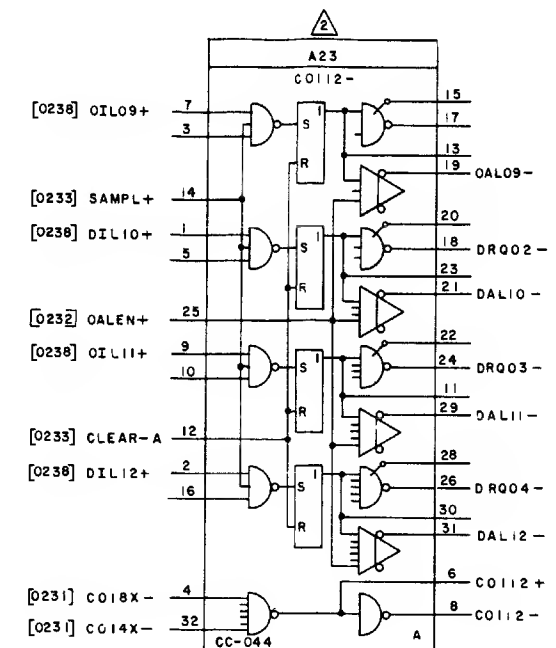
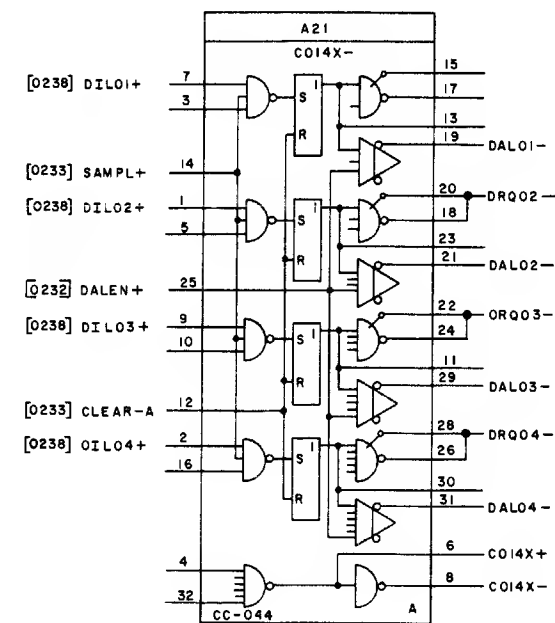
Figure 5. Cable Assembly, Special Purpose

Fig. & Index No.	Designation	CCD Part No.	Description	Qty. per Assy.
5-	A1A507, A1A508	013826701	CABLE ASSEMBLY (Refer to Figure 4 for NHA.)	Ref.
-1		014998701	PRINTED CIRCUIT CARD (Jumper PAC)	2
-2		940404001	CABLE, FLAT, MULTI-CONDUCTOR -34 conductor, equivalent to 32 AWG, 1.80 in. width, .014 in. thk.	A/R

## LOGIC BLOCK DIAGRAMS

Logic block diagrams (listed below) for the H316-20 DMC option follow.

<u>LBD No.</u>	<u>Title</u>	<u>Dwg. No.</u>
0. 231	H316 SDMC Priority Net	70025578
0. 232	H316 SDMC Cycle TLG	70025579
0. 233	H316 SDMC Control	70025580
0. 234	H316 SDMC M-Register Storage	70025581
0. 235	H316 SDMC M-Register Input	70025582
0. 236	H316 SDMC Address Register	70025583
0. 237	H316 SDMC Comparator IYB	70025584
0. 238	H316 SDMC Cable and Out Bus	70025585
0. 239	PAC Comp/Alloc	70025577



NOTES:

- 1 INSTALL IF MORE THAN 4 CHANNELS
- 2 INSTALL IF MORE THAN 8 CHANNELS
- 3 INSTALL IF MORE THAN 12 CHANNELS
- 4

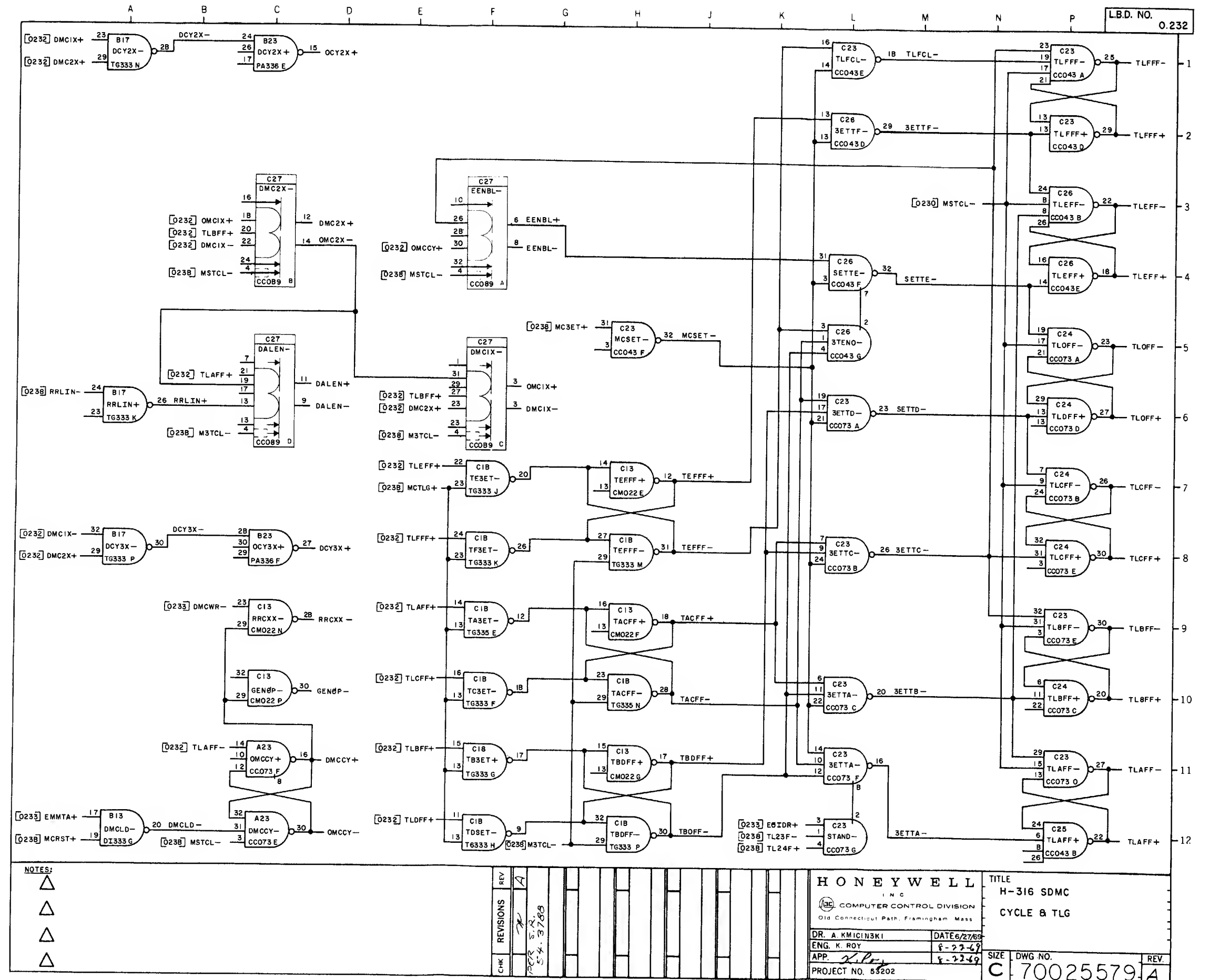
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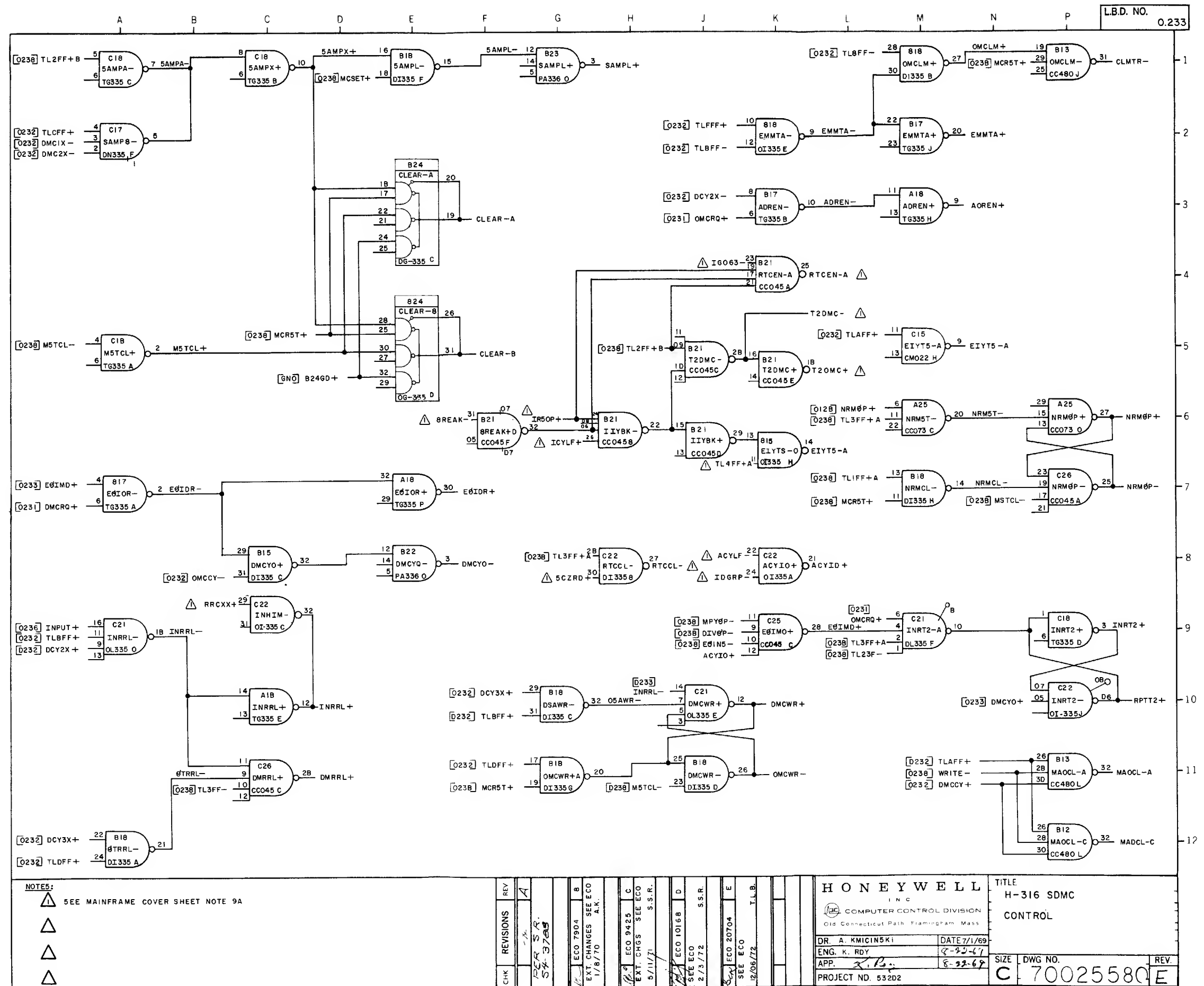
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INC  
 **COMPUTER CONTROL DIVISION**  
Old Connecticut Path, Framingham, Mass.

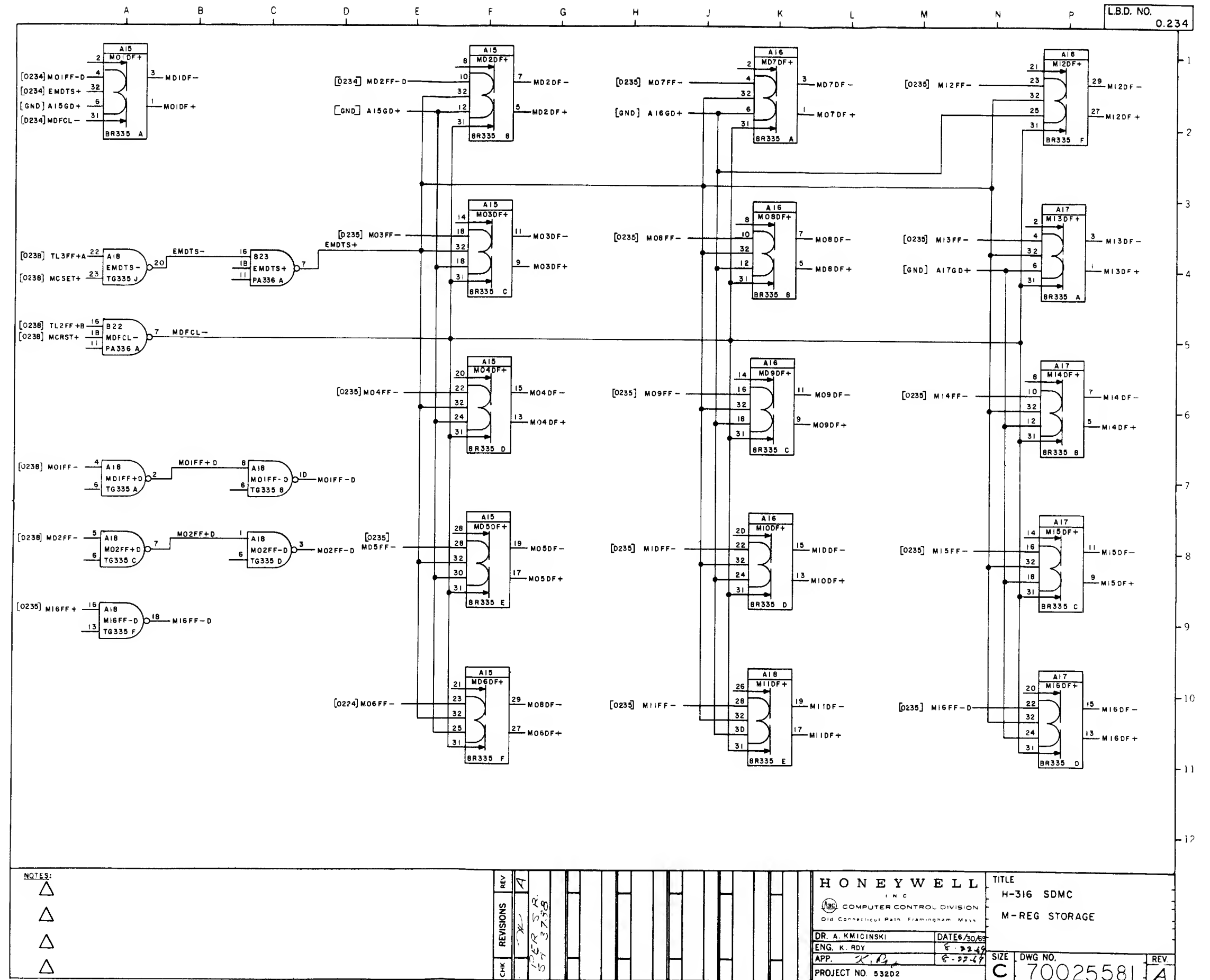
DR. A. KMICINSKI	DATE 6/27/8
ENG. K ROY	8-22-69
APP. <i>X. Roy</i>	8-22-69
PROJECT NO 53202	

TITLE
H-316 SDMC
PRIORITY NET

SIZE	DWG NO.	REV.
C	70025578	A

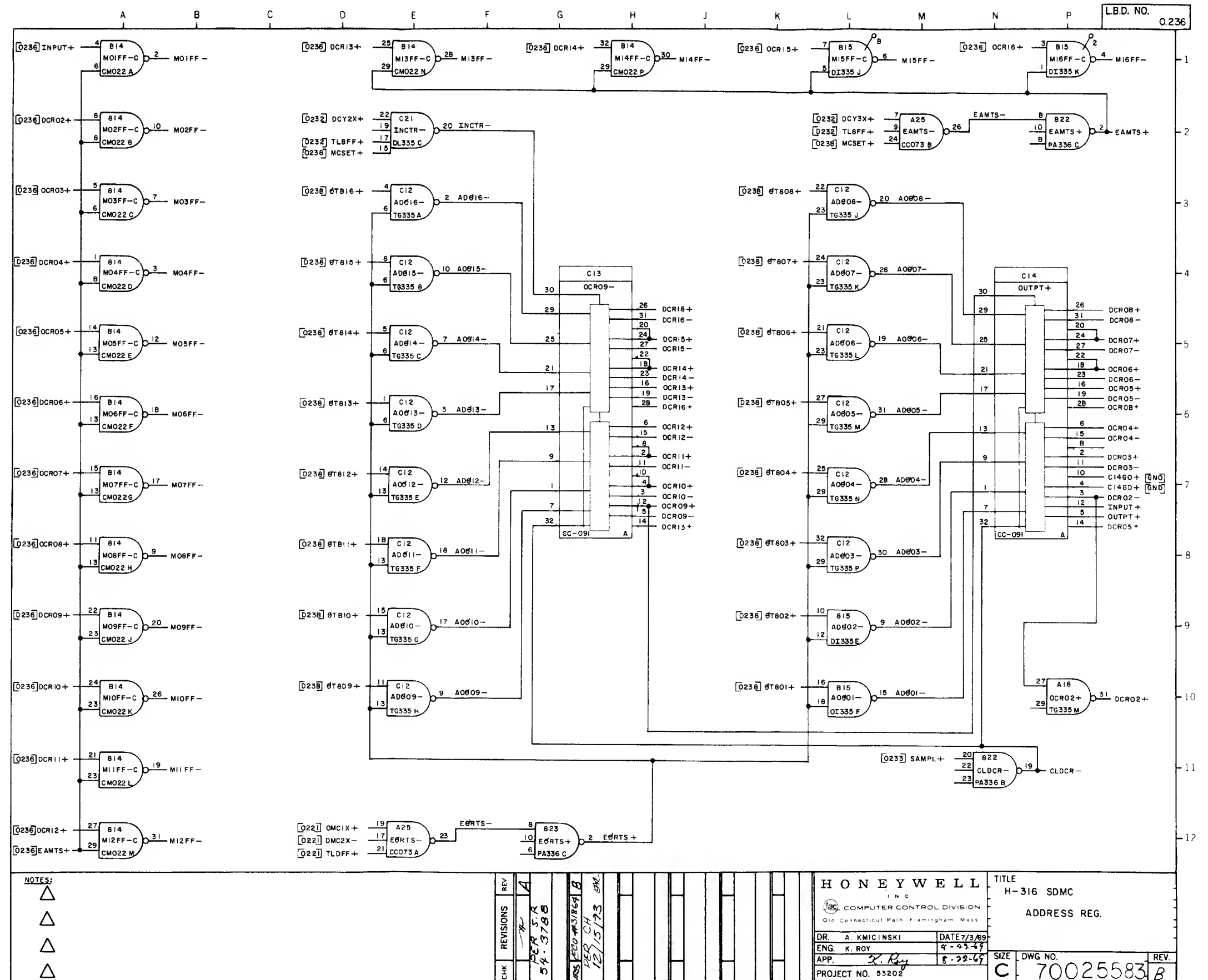


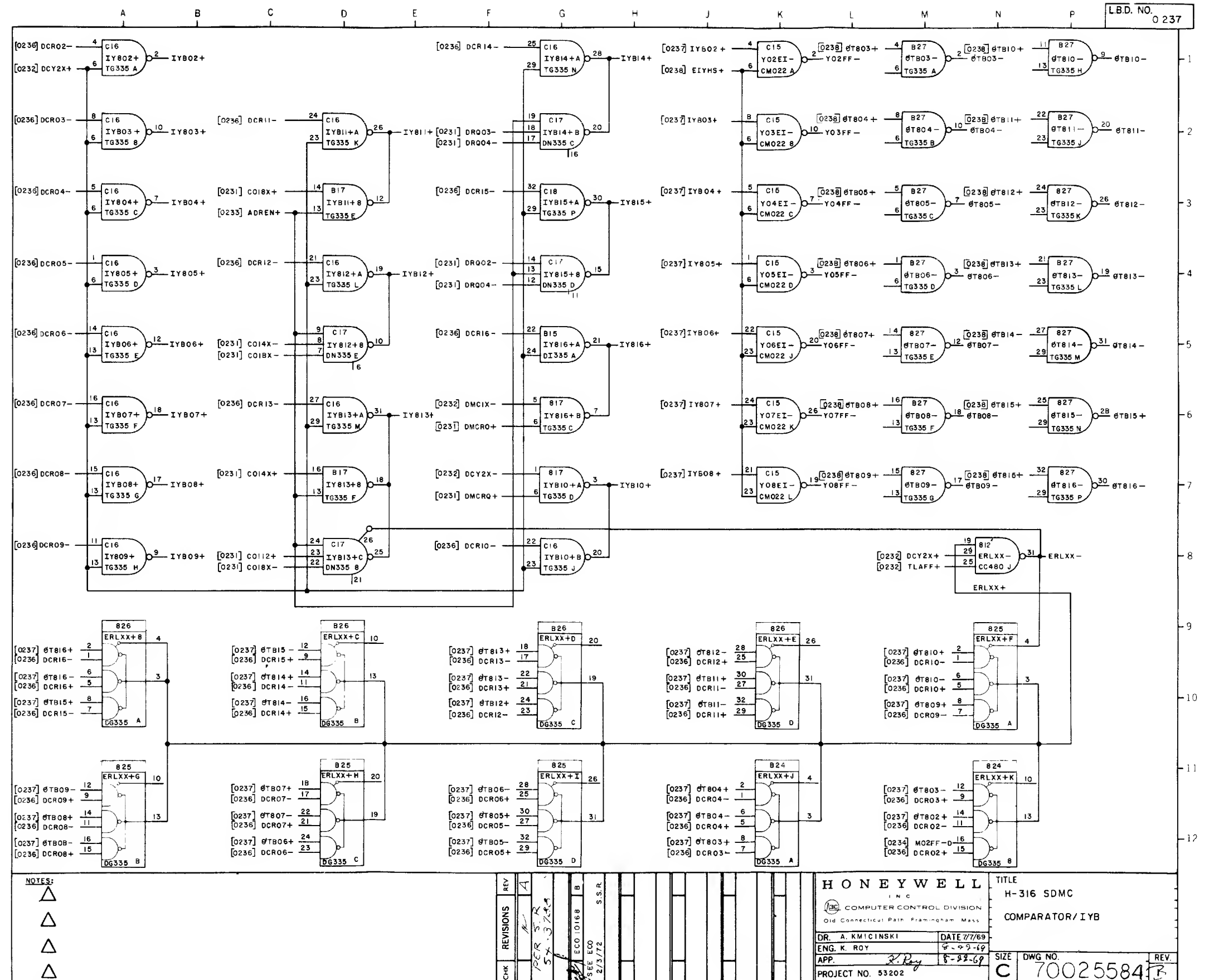


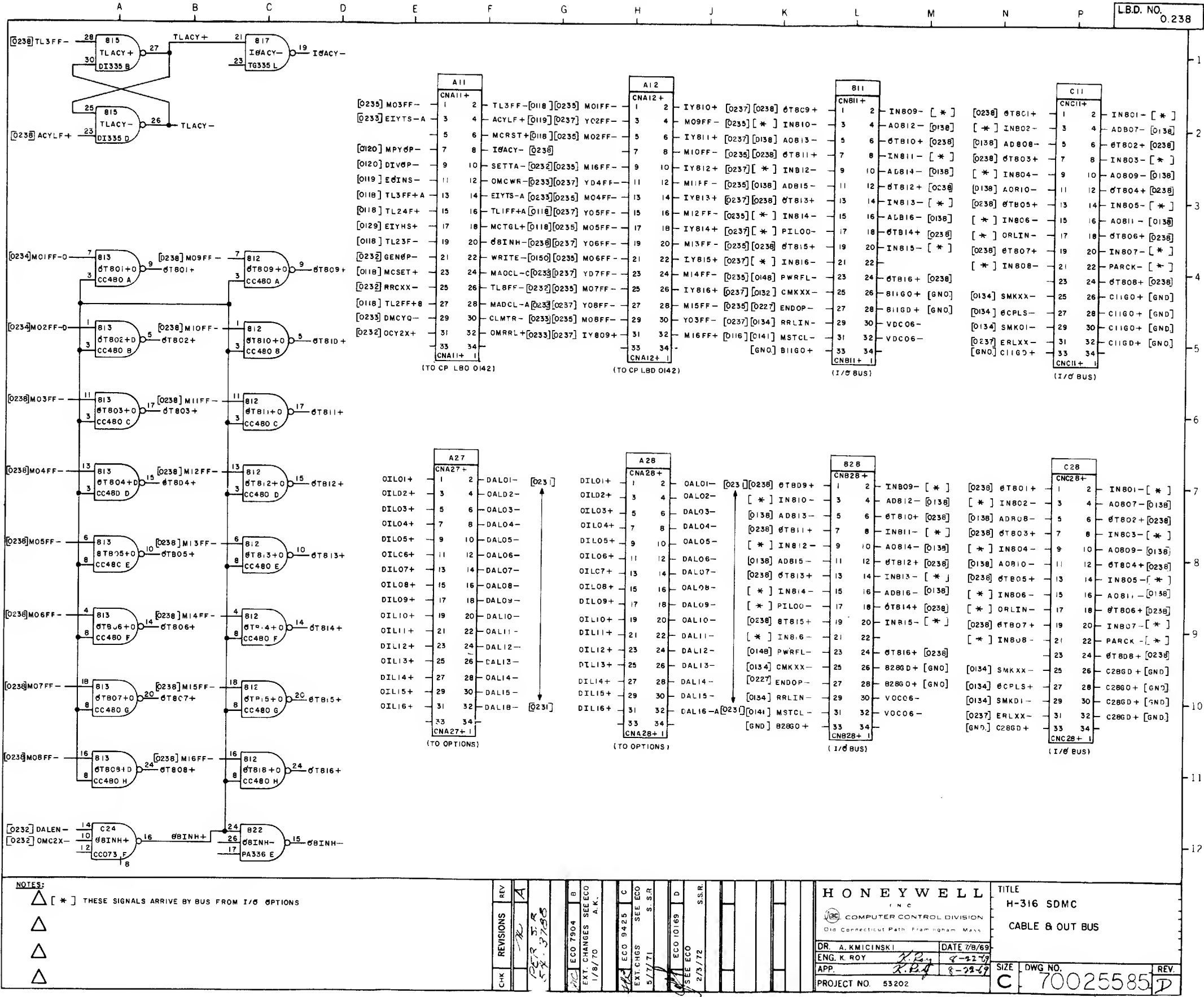












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REVISIONS  
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ECO 7904  
EXT. CHGS. SEE ECO  
A.K.

ECO 9425  
EXT. CHGS. SEE ECO  
5/7/71

ECO 10238  
EXT. CHGS. SEE ECO  
3/10/72

ECO 20704  
SEE ECO  
12/06/72

T.L.B.

P70025577  
3C DRAWING NUMBER

PARTS LIST  
DESCRIPTION

HONEYWELL  
IN C.  
COMPUTER CONTROL DIVISION  
Old Connecticut Path, Framingham, Mass.

DR. A. KMICINSKI  
ENG. K. ROY  
APP. *K.R.*

DATE 7/9/69  
8-22-69  
8-22-69

TITLE  
PAC COMP/ALLOC

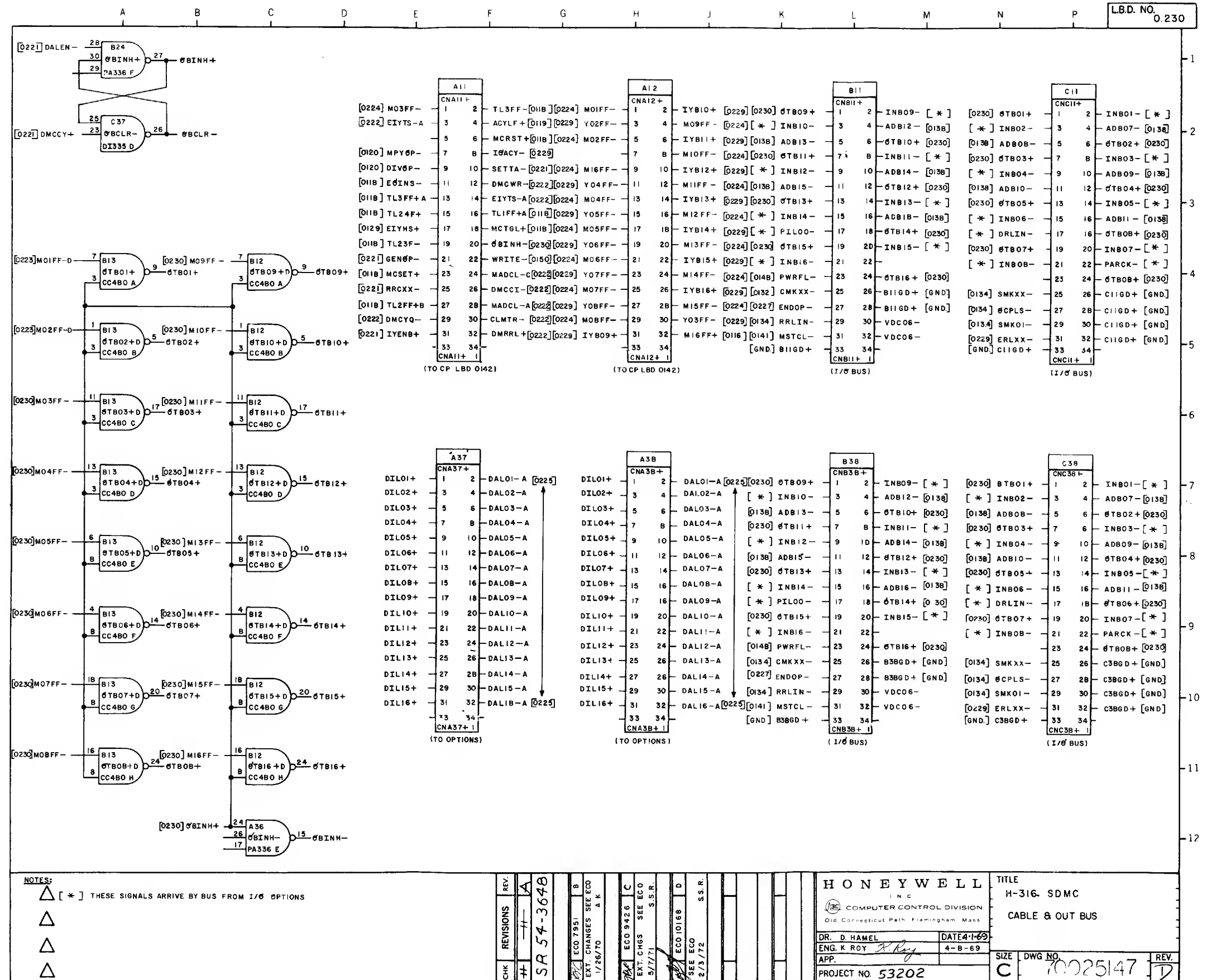
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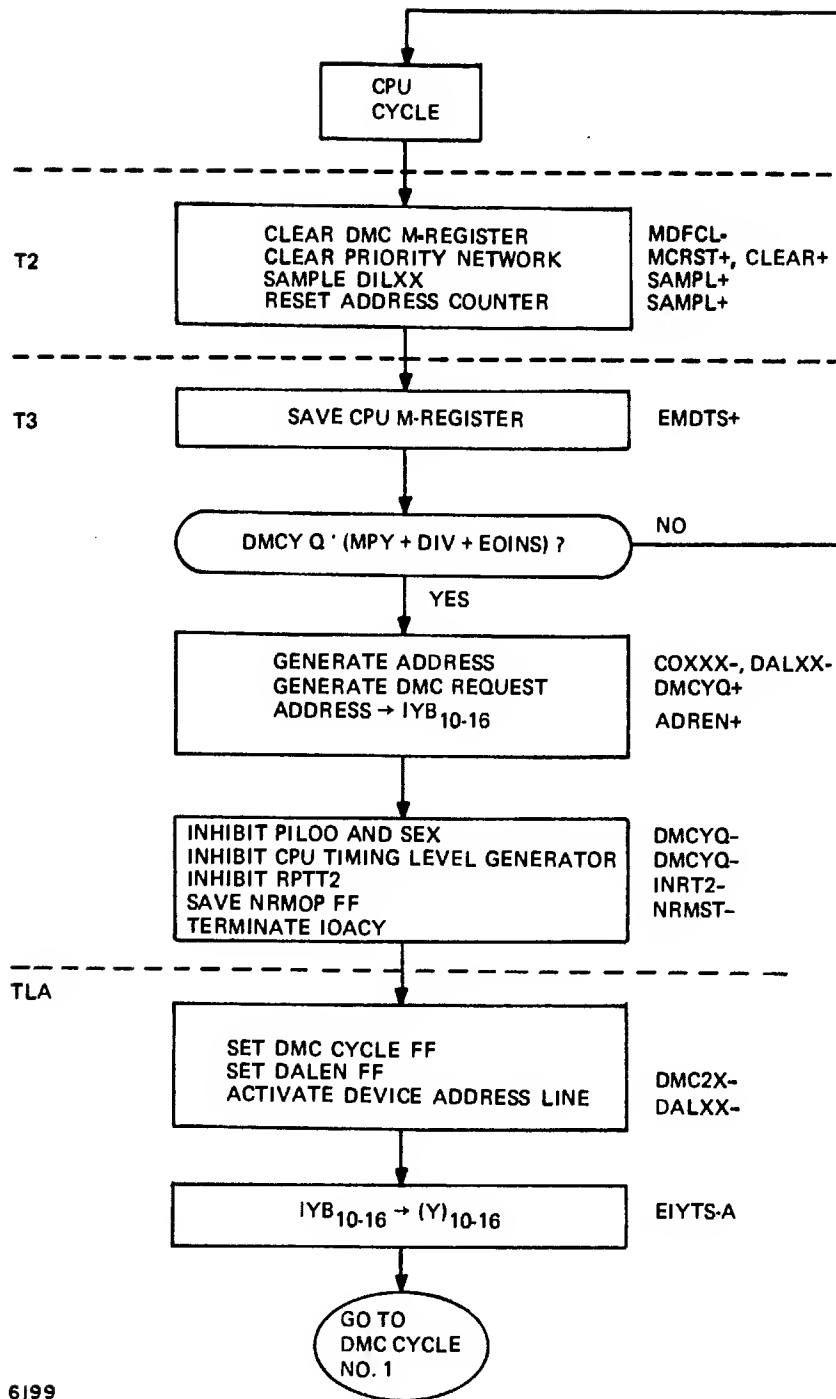
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33



APPENDIX A  
FLOW CHARTS AND ANALYSES



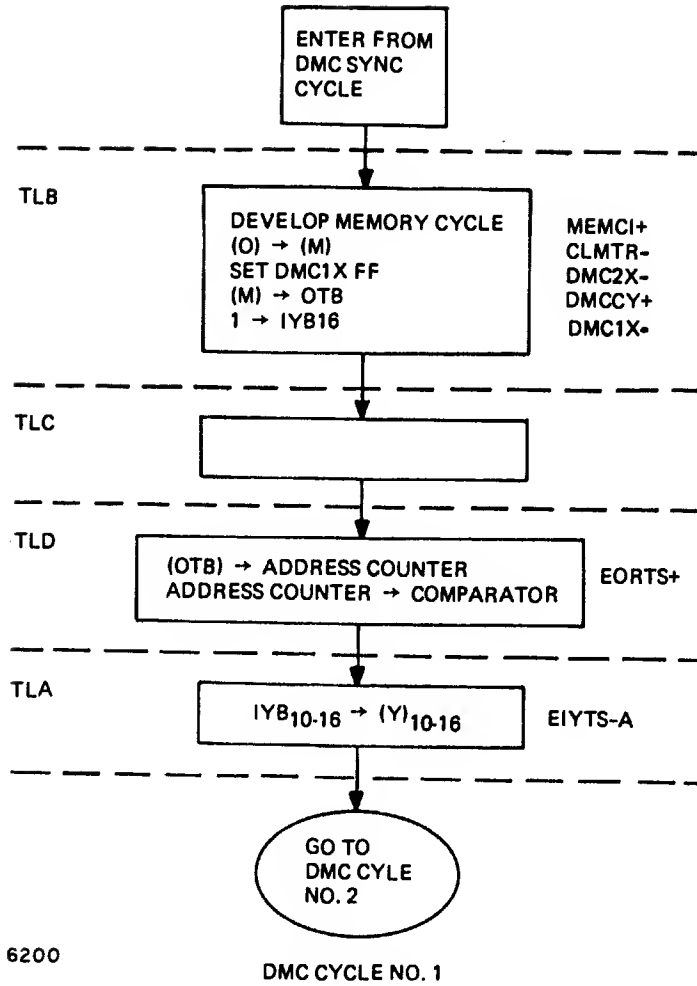
6199

DMC SYNC CYCLE

DMC Sync Cycle

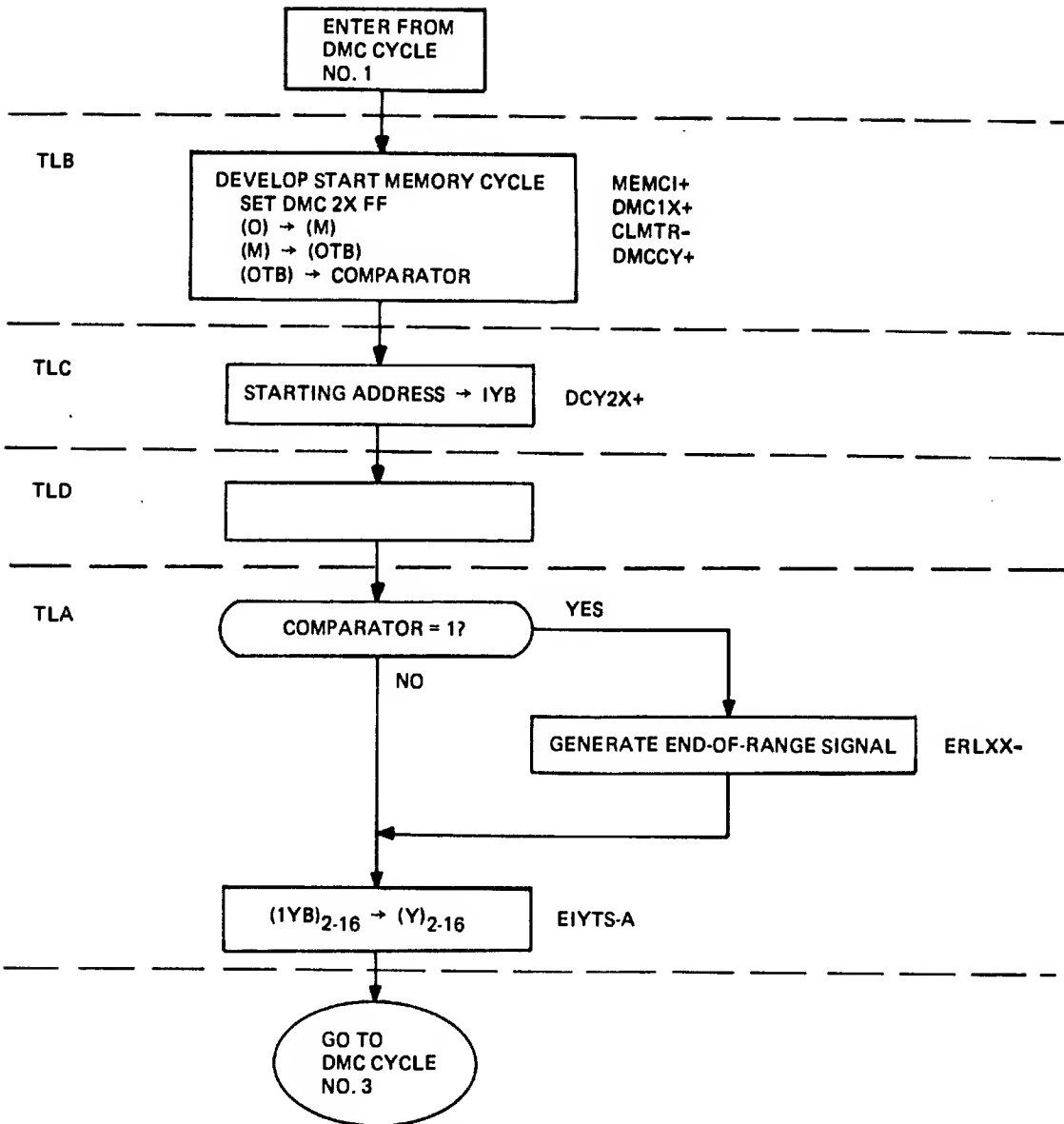
Signal	Origin	Cyc	Time	Clk	Signal Component	Origin	Destination	Operation Description
CLEAR-	233-E4	CPU	T2		(SAMPX+)(MCRST+)	233-C1	231-B4/ B10 K4/ K10	Clears PN
MDFCL-	234-B5	CPU	T2		(MCRST+)(TL2FF+)	234-A5	234	Clear DMC M-Register
SAMPL+	233-H1	CPU	T2		(SAMPX-)(MCSET+)	233-D1	231-A2/ K2/ A8/ K8	Enable active DILXX requests to set associated PN channel flip-flops which generate DRQXX- and COXXX- signals
DIL01+ thru DIL16+	External Device						236/N11	Clear Address Counter
EMDTS+	234-C4	CPU	T3		(MCSET+)(TL3FF)	234-A4	231	Data transfer request to PN
COXXX-	231	CPU	T3		(SAMPL+)(DILXX+)	231	234	Save CPU M-register
DRQXX-							231-F7	Generate DMC RQ+
							237-C/ G	Generate most significant portion of starting address location in IYBXX+ lines
DMCYQ+	233-F8	CPU	T3		(EOIDR-)(DMCCY-)	233-B8	233	Generate DMC request
ADREN+	233-N3	CPU	T3		(DMCRQ+)(DCY2X-)	233-J3	237-C3	Enables PN Address to IY bus
INRT2-	233-M9	CPU	T3		(DMCRQ+)(EOIMD+) (TL3FF+)(TL23F-)	233-L9	233-P10	Inhibit RPTT2
NRMST-	233-M6	CPU	T3		(NRMOP+)(TL3FF+)	233-L6	233-P6	Save NRMOP
DALEN+	232-C6	DMC	TLA		(TLAFF+)(DMC2X-)	232-B6	231	Set DAL Lines
DALXX	231	DMC	TLA		(DALEN+)(DILXX)	231	238	Device Address Lines
DMCCY+	232-C11	DMC	TLA		(TLAFF-)	232	232-E5 233-P11 238-A/ B	Reset EENBL Enable DMC MADCL Enable DMC OTB
EIYTS-A	233-M5	DMC	TLA		(TLAFF+)	233	238-D2	Gates IY bus bits 10-16 to Y-register 10-16





DMC Cycle No. 1

Signal	Origin	Cyc	Time	Clk	Signal Component	Origin	Destination	Operation Description
CLMTR-	233-P1	DMC	TLB		(DMCLM+)(MCRST+)	233-N1	238-F4	Clears M-register
DMC1X+	232-F5	DMC	TLB		(DMC2X-)(TLBFF+)	232-E5	237-F6	Puts a ONE on IYB16+ as the final address is odd
MEMCI+	126-K12	DMC	TLB		(TLBFF-)	238-F4		Initiates memory cycle
EORTS+	236-G12	DMC	TLD		(DMC1X+)(DMC2X-)(TLDFF+)	236-D12	236	Enables output bus to address counter
EIYTS-A	233-M5	DMC	TLA		(TLAFF+)	233-M5	238-E2	Gates IY bus bits 10-16 to Y-register bits 10-16

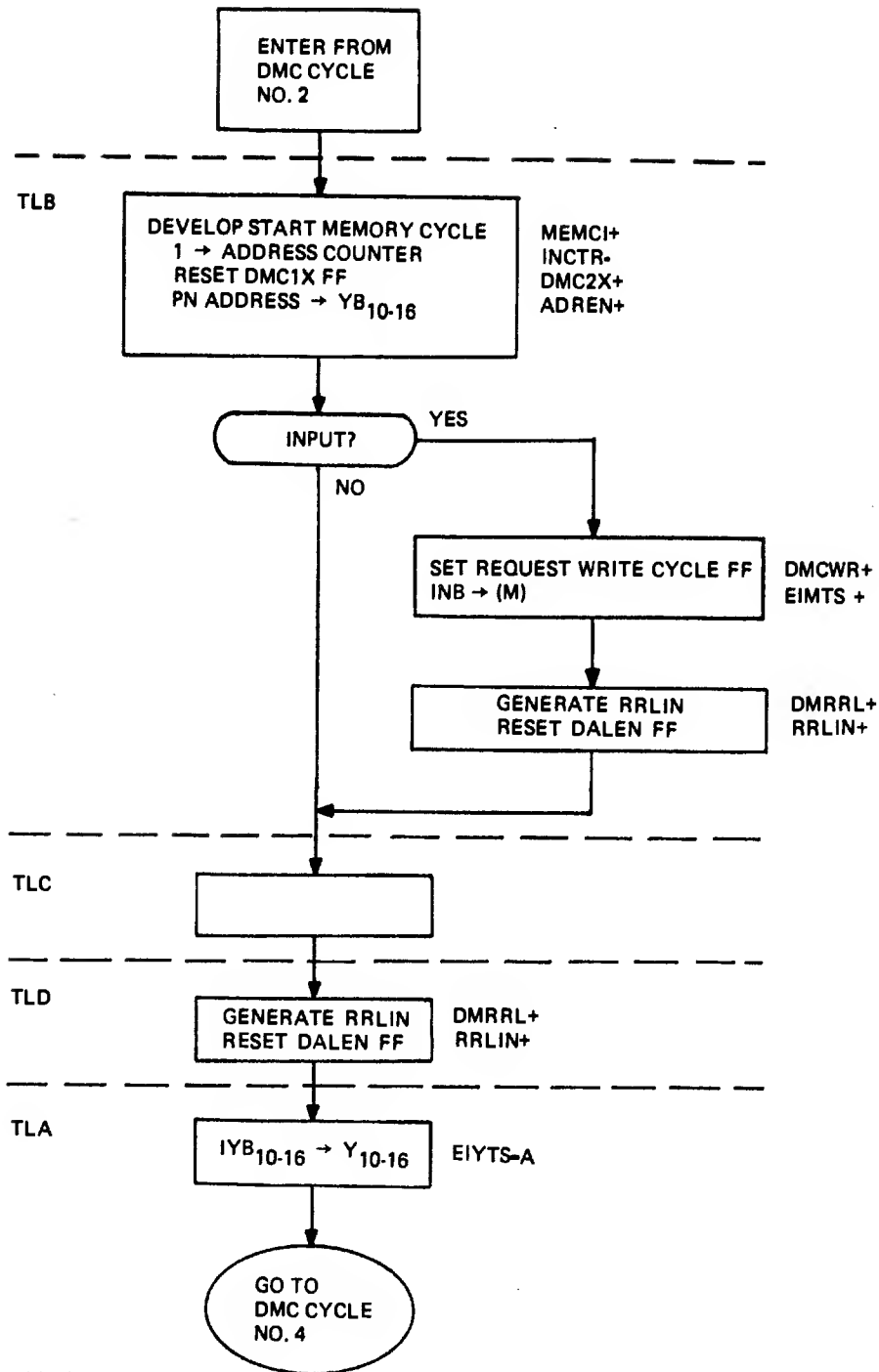


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DMC CYCLE NO. 2

DMC Cycle No. 2

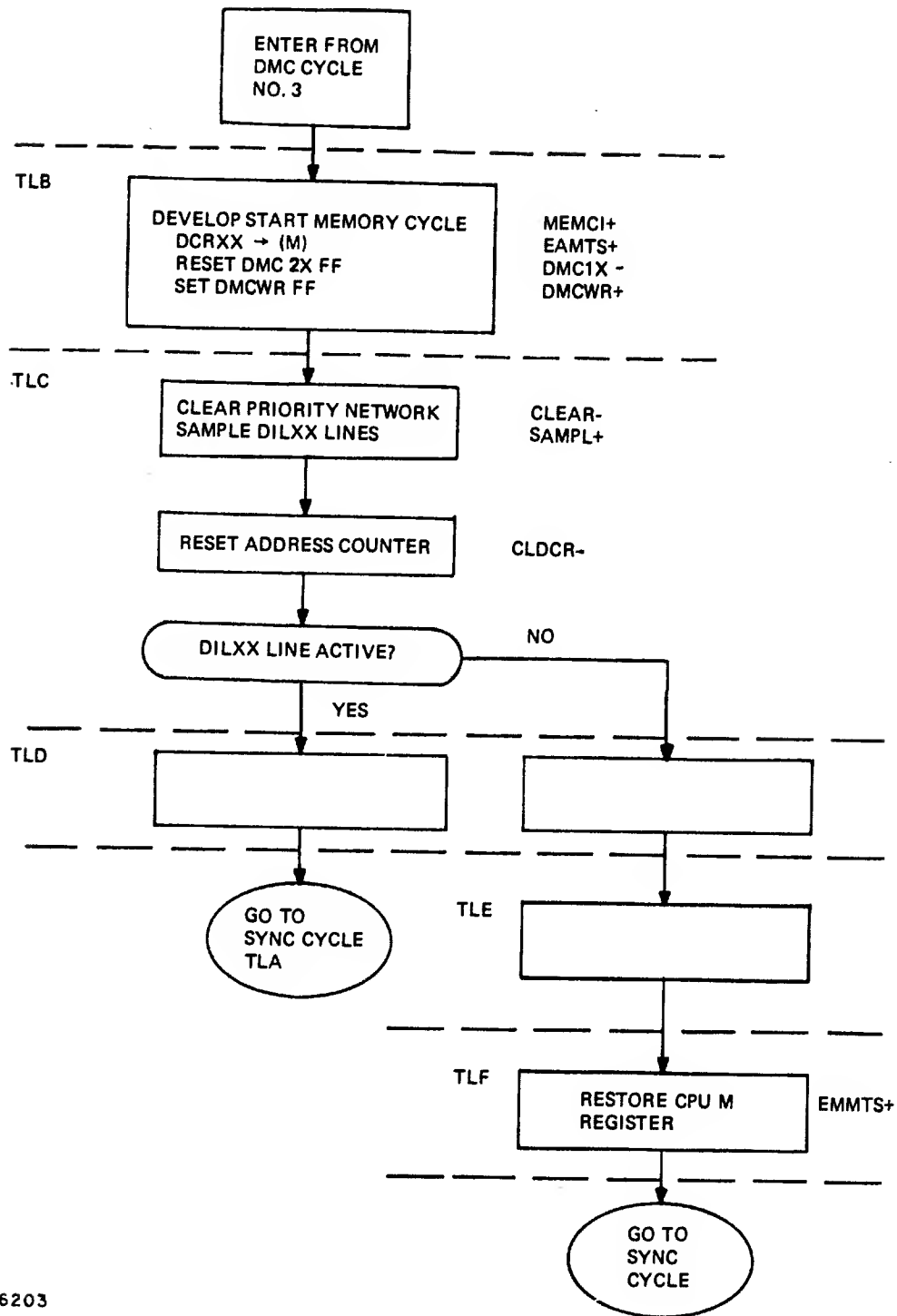
Signal	Origin	Cyc	Time	Clk	Signal Component	Origin	Destination	Operation Description
MEMCI+	126-K12	DMC	TLB		(TLBFF-)			Initiate memory cycle
DMC2X+	232	DMC	TLB		(DMC1X+)(TLBFF+)	232-B3	232-E6 232-A1	Enable reset DMC1X Generate DCY2X+
CLMTR-	233-P1	DMC	TLB		(DMCLM+)(MCRST+)	233-N1	238-F4	Clears M-register
DCY2X+	232-C1	DMC	TLB		(DMC1X+)(DMC2X+)	232-A1	237-N8 236-E2 233-A9 237	Enable ERLXX- Enable increment address counter Enable RRL input mode gate address counter to IY bus
EIYTS-A	233-M5	DMC	TLA		(TLAFF+)	233-M5	238-E2	Gates IY bus bits 10-16 to Y-register bits 10-16
EIYHS+	129-P6	DMC	TLA		(DCY2X+)(MCSET+) (EIYTS+)	232-C2	109-P12 237-K	Gates IY bus bits 2-9 to Y-register bits 2-9
ERLXX-	237-P8	DMC	TLA		(DCY2X+)(TLAFF+) (ERLXX+)	237-M8	238-P5 238-P10	Enable end of range to device



DMC CYCLE NO. 3

DMC Cycle No. 3

Signal	Origin	Cyc	Time	Clk	Signal Component	Origin	Destination	Operation Description
INCTR-	236-E2	DMC	TLB		(DCY2X+)(TLBFF+)	236-D2	236-G4	Increment address counter by 1
MEMCI+	126-K12	DMC	TLB		(MCSET+)(TLBFF-)			Initiate memory cycle to readout or store data words
ADREN+	233-N3	DMC	TLB		(DMCRQ+)(DCY2X-)	233-J3	237-C3	Enables PN address to IY bus
EIMTS+	235-C10	DMC	TLB		(INRRL+)(MCSET+)	235-A10	235-G11	Enables IYB to M-register
DMCWR+	233-K10	DMC	TLB		(TLBFF+)(INRRL-)	233-B9		Set DMCWR
DCY3X+	232-C8	DMC	TLB		(DMC1X-)(DMC2X+)	232-A8	236-L2	Gates incremented address register to M-register
DMC1X-	232-F6	DMC	TLB		(DMC2X+)(TLBFF+)	232-C3	232-A1 232-A8	Disable DCY2X+ Generate DCY3X+
DMRRL+	233-C11	DMC	TLB		(INPUT+)(DCY2X+)(TLBFF+)	233-A8	134-P10	Enable RRL in Input mode
RRLIN+	232-A6	DMC	TLB		(RRLIN-)	134-P10	232-C6	Reset DALEN in Input mode
DMRRL+	233-C1	DMC	TLD		(DCY3X+)(TLDFF)	233-A8	134-P10	Enable RRL in Output mode
RRLIN+	232-A6	DMC	TLD		(RRLIN-)	134-P10	232-C6	Reset DALEN in Output mode
EIYTS-A	233-M5	DMC	TLA		(TLAFF+)	233-M5	238-E2	Gates IY bus bits 10-16 to Y-register bits 10-16



6203

DMC CYCLE NO. 4

DMC Cycle No. 4

Signal	Origin	Cyc	Time	Clk	Signal Component	Origin	Destination	Operation Description
MEMCI+	126-K12	DMC	TLB		(TLBFF-)			Initiate memory cycle
EAMTS+	236-P2	DMC	TLB		(DCY3X+)(TLBFF+) (MCSET+)	236-M2	236-A1-12 236-A1-P1	Enables address counter to CPU M-register
DMCWR+	233-K10	DMC	TLB			233-F11		Sets DMCWR flip-flop
DMC2X-	232-C3	DMC	TLB		(DMC1X-)(TLBFF+)	232-C3	232-A6	Disables DCY3X+
CLEAR-	233-E3	DMC	TLC		(SAMPX+)(MCRST+)	233-L5	231-B4/ B10 K4	Clears priority network
SAMPL+	233-H1	DMC	TLC		(SAMPX+)(MCSET+)	233-D1	231-A2/K2 A8 K8	Enables active DILXX request to set associated PN channel flip-flops which generate DRQXX- and COXXX- signals
CLDCR-	236-P11	DMC	TLC		(SAMPL+)	233-H1	236-M11	Clear address register
EMMTS+	235-D12	DMC	TLF		(EMMTA+)(MCSET+)	235-A12	235-B7	Restores M-register to CPU



APPENDIX B  
SPECIAL PAC DESCRIPTIONS

Descriptions of the following special PACs (listed below) are presented in this Appendix.

CC-044  
CC-045  
CC-073  
CC-089  
CC-091  
CC-480

## PRIORITY PAC, MODEL CC-044

### GENERAL DESCRIPTION

The Priority PAC, Model CC-044 (Figure 1), contains five F-01, two F-02, and two F-03 microcircuits. They are interconnected to perform the priority function in a digital computer.

### SPECIFICATIONS

#### Frequency of Operation

DC to 5 MHz

#### Input Loading

1 unit load per F-01 gate

1 unit load per F-02 gate

2 unit loads per F-03 amplifier

#### Output Drive Capability

##### Pins

##### Unit Loads Each

19, 21, 29, 31 25

8, 17, 18, 24, 28 8

6 7

11, 13, 23, 30 4

#### Circuit Delay (measured at +1.5v, averaged over two stages):

30 ns (max)

#### Current Requirements

+6v: 160 ma (max)

#### Power Dissipation

0.96w (max)

### Electrical Parts List

Ref. Desig.	Description	Part No.
M1, M5, M7-M9	MICROCIRCUIT: F-01, dual NAND gate integrated circuit	950 100 001
M2, M6	MICROCIRCUIT: F-02, quad NAND gate integrated circuit	950 100 002
M3, M4	MICROCIRCUIT: F-03, power amplifier integrated circuit	950 100 003
C1	CAPACITOR, FIXED, PLASTIC DIELECTRIC: 0.033 $\mu$ f $\pm$ 20%, 50 vdc	930 313 016
CR1-CR19	DIODE	943 083 001

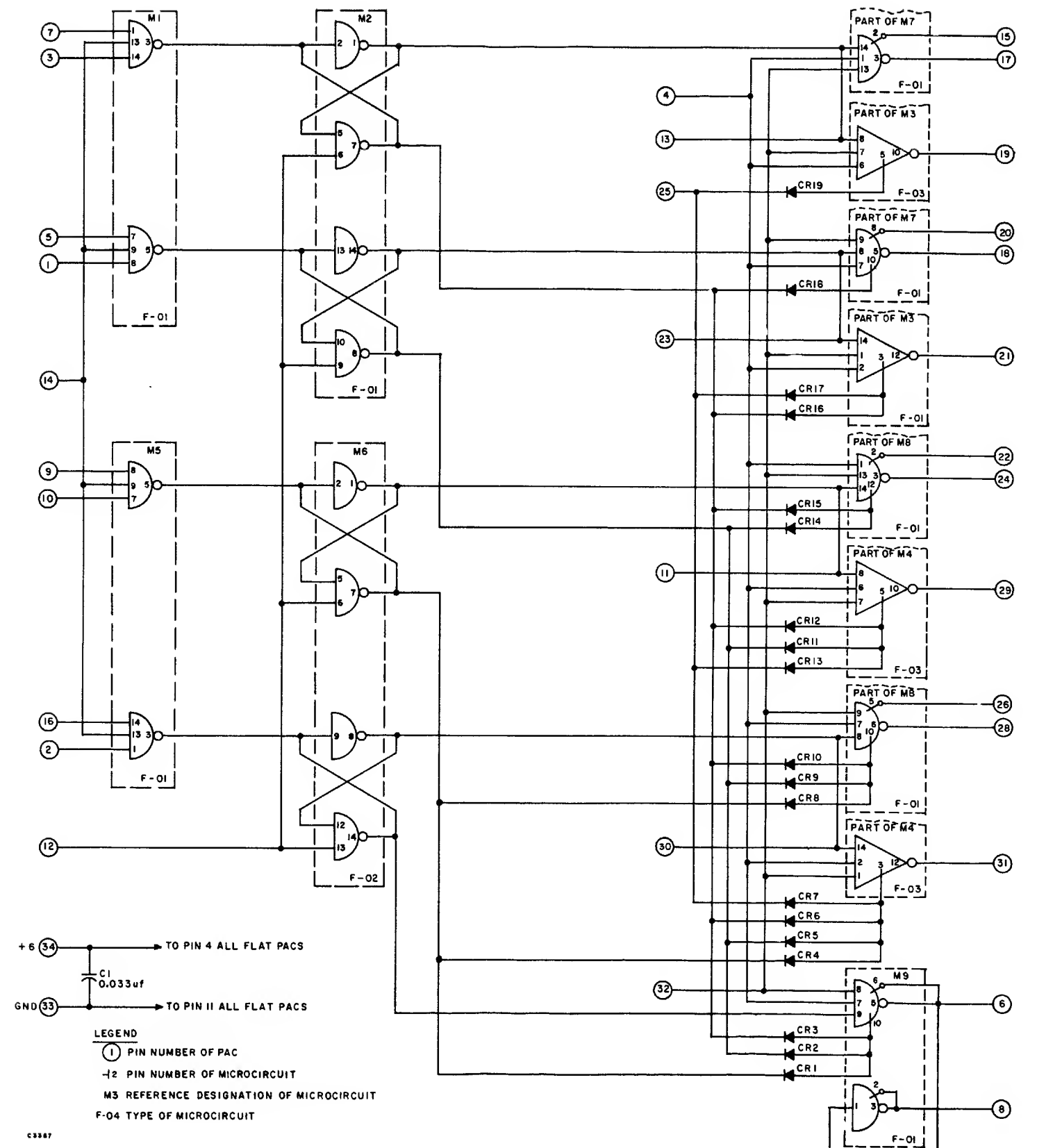


Figure 1. Priority PAC, Model CC-044, Schematic Diagram

## NAND TYPE I POWER AMPLIFIER PAC, MODEL CC-045

## GENERAL DESCRIPTION

The NAND Type I Power Amplifier PAC, Model CC-045 (Figure A-28), contains three 4-input and three 2-input NAND gates that can be used to drive heavy loads. One of the 2-input gates has a node connected to pin 7 which can be used for input expansion. A three-diode cluster is also provided for expansion of input gating. Built-in short circuit protection limits the output current if the output is accidentally grounded.

## CIRCUIT FUNCTION

Each gate performs the NAND function for positive logic and the NOR function for negative logic. When all inputs to a gate are positive or not connected, the output will be at ground. If any input is at ground, the output goes to a positive voltage.

## NOTE

The following pins must be jumpered together on the connector into which a CC-045 is inserted. These jumpers should be made as short as possible.

Pin 20 to pin 33  
Pin 27 to pin 30  
Pin 30 to pin 33

## SPECIFICATIONS

Frequency of Operation

DC to 10 MHz

Input Loading

2 unit loads

Current Requirements

+6v - 90 ma (max)

Power Dissipation

0.54w (max)

Output Drive Capability

12 unit loads and 70 pf stray capacitance, or  
25 unit loads and 250 pf stray capacitance

Circuit Delay (measured at +1.5v, averaged over two stages)

15 ns (max) with 12 unit loads and 70 pf load  
30 ns (max) with 25 unit loads and 250 pf load

## Electrical Parts List

Ref. Desig.	Description	3C Part No.
M1-M3	MICROCIRCUIT: F-09, power amplifier integrated circuit	950 100 009
C1	CAPACITOR, FIXED, PLASTIC DIELECTRIC: 0.033 $\mu$ f $\pm$ 20%, 50 vdc	930 313 016
CR1-CR3	DIODE	943 083 001

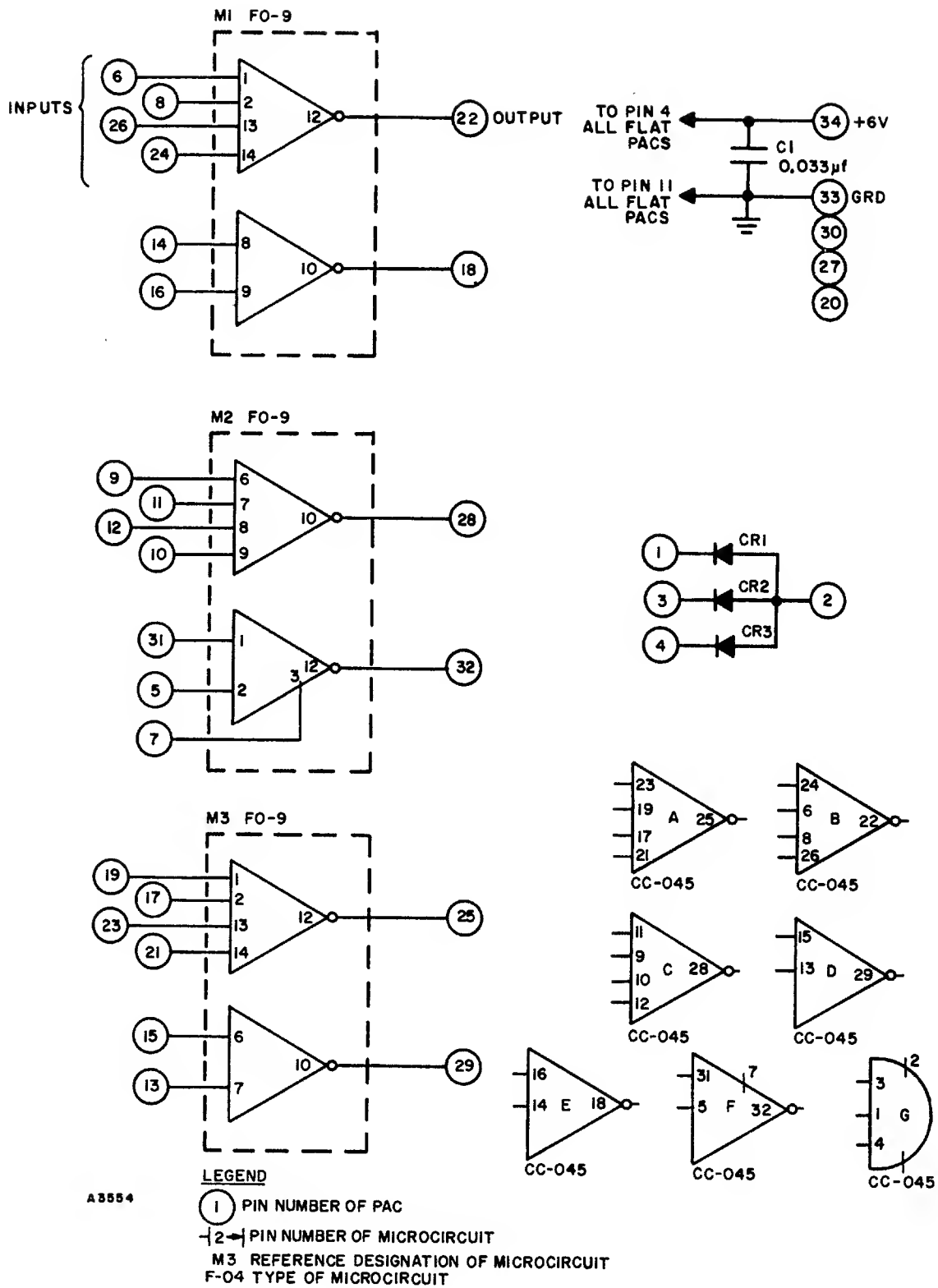


Figure A-28. NAND Type I Power Amplifier PAC, Model CC-045, Schematic Diagram and Logic Symbol

## NAND TYPE II POWER AMPLIFIER PAC, MODEL CC-073

### GENERAL DESCRIPTION

The NAND Type II Power Amplifier PAC, Model CC-073 (Figure A-32), contains six 3-input NAND gates that can be used to drive heavy loads. One of the gates has a node connected to pin 8 which can be used for input expansion. A three-diode cluster is also provided for expansion of input gating. Built-in short circuit protection limits the output current if the output is accidentally grounded.

### CIRCUIT FUNCTION

Each gate performs the NAND function for positive logic and the NOR function for negative logic. When all inputs to a gate are positive or not connected, the output will be at ground. If any input is at ground, the output goes to a positive voltage.

#### NOTE

The following pins must be jumpered together on the connector into which a CC-073 is inserted. These jumpers should be made as short as possible.

From pin 18 to pin 33  
From pin 25 to pin 28  
From pin 28 to pin 33

### SPECIFICATIONS

<u>Frequency of Operation</u>	<u>Current Requirements</u>
DC to 10 MHz	+6v: 90 ma (max)
<u>Output Drive Capability</u>	<u>Power Dissipation</u>
12 unit loads and 70 pf stray, or 25 unit loads and 250 pf stray	0.54w (max)
<u>Input Loading</u>	
2 unit loads	
<u>Circuit Delay</u> (measured at +1.5v, averaged over two stages)	
15 ns (max) with 12 unit loads and 70 pf load	
30 ns (max) with 25 unit loads and 250 pf load	

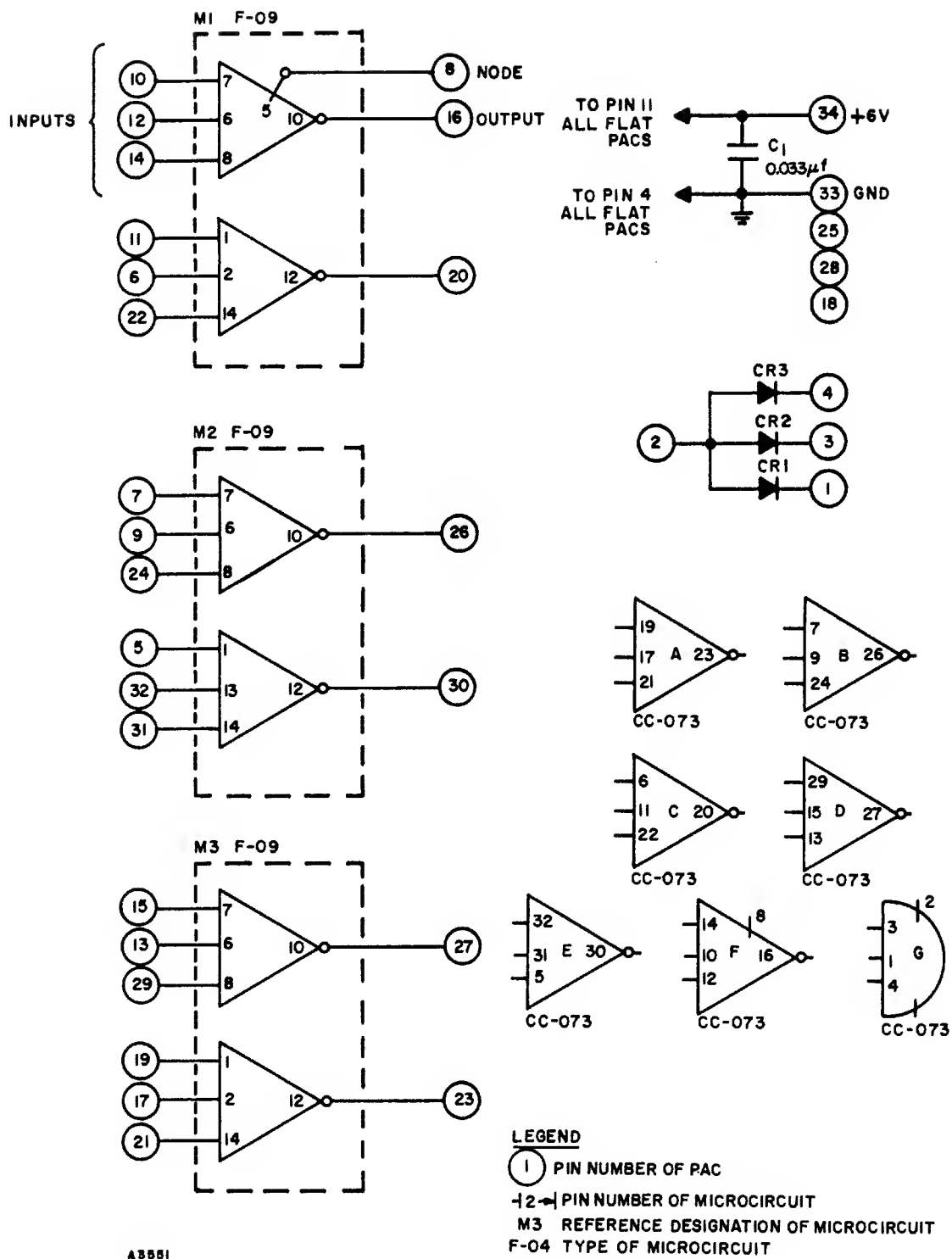


Figure A-32. NAND Type II Power Amplifier PAC, Model CC-073, Schematic Diagram and Logic Symbols

# Electrical Parts List

Ref. Desig.	Description	3C Part No.
M1-M3	MICROCIRCUIT: F-09, power amplifier integrated circuit	950 100 009
C1	CAPACITOR, FIXED, PLASTIC DIELECTRIC: 0.033 $\mu$ f $\pm$ 20%, 50 vdc	930 313 016
CR1-CR3	DIODE	943 083 001



## GATED FLIP-FLOP PAC, MODEL CC-089

The Gated Flip-Flop PAC, Model CC-089 (Figures A-50 and A-51), contains four independent flip-flops. A versatile input structure allows control from a variety of levels and pulses. Typical applications are storage, counting and shifting, and control.

### INPUT AND OUTPUT SIGNALS

DC Set and DC Reset. -- A signal at 0v for 80 nsec or longer on a dc set (or reset) input will set (or reset) the flip-flop.

Common Reset. -- A signal at 0v for 80 nsec or longer on the common reset input clears all four stages simultaneously.

Set Control and Reset Control. -- +6v is the enabling level on the control inputs.

Clock. -- The flip-flop changes state on the negative transition of the clock input.

### SPECIFICATIONS

<u>Frequency of Operation (System)</u>	<u>Circuit Delay</u>
DC to 5 mc	Clock input to set or reset output: 60 nsec (max)
<u>Input Loading</u>	DC set input to dc set output, or dc reset input to reset output: 80 nsec (max)
DC inputs: 2/3 unit load each	DC set input to reset output, or dc reset input to set output: 60 nsec (max)
Control inputs: 1 unit load each	<u>Current Requirements</u>
Common reset: 3 unit loads	+6v: 100 ma (max)
Clock: 1 unit load each	<u>Power Dissipation</u>
<u>Output Drive Capability</u>	0.60w (max)
8 unit loads each	<u>Handle Color Code</u>
	Blue

### APPLICATIONS

The CC-089 can be used as a counter (Figure A-52) or as a shift register (Figure A-53). The method of parallel information drop-in is shown in Figure A-54.

Data may be transferred to the flip-flop with a single-ended signal by first resetting all stages, then setting the appropriate ones. For double-ended data transfer, complementary signals applied to the dc set and dc reset inputs set the flip-flop to the appropriate state in one operation.

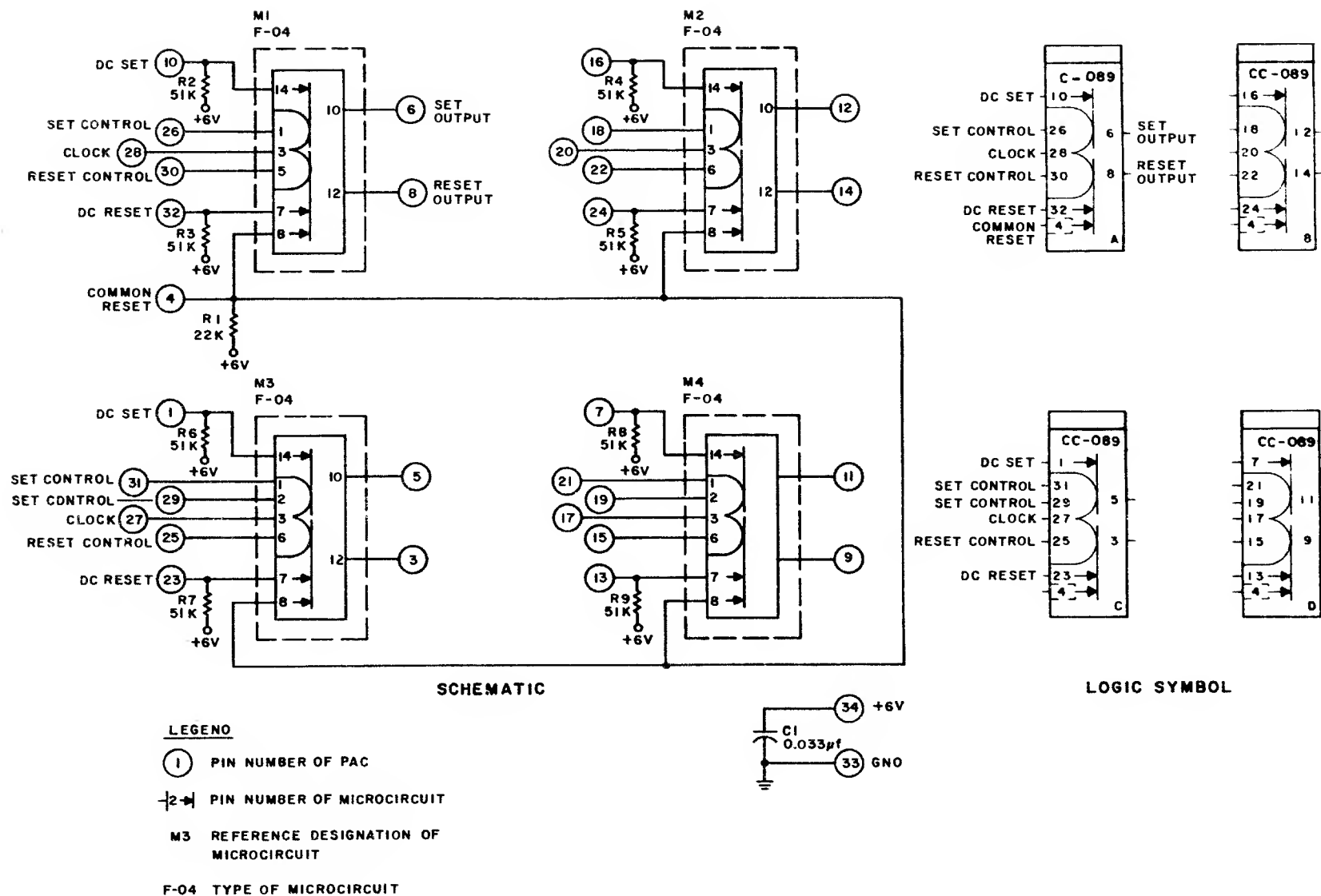
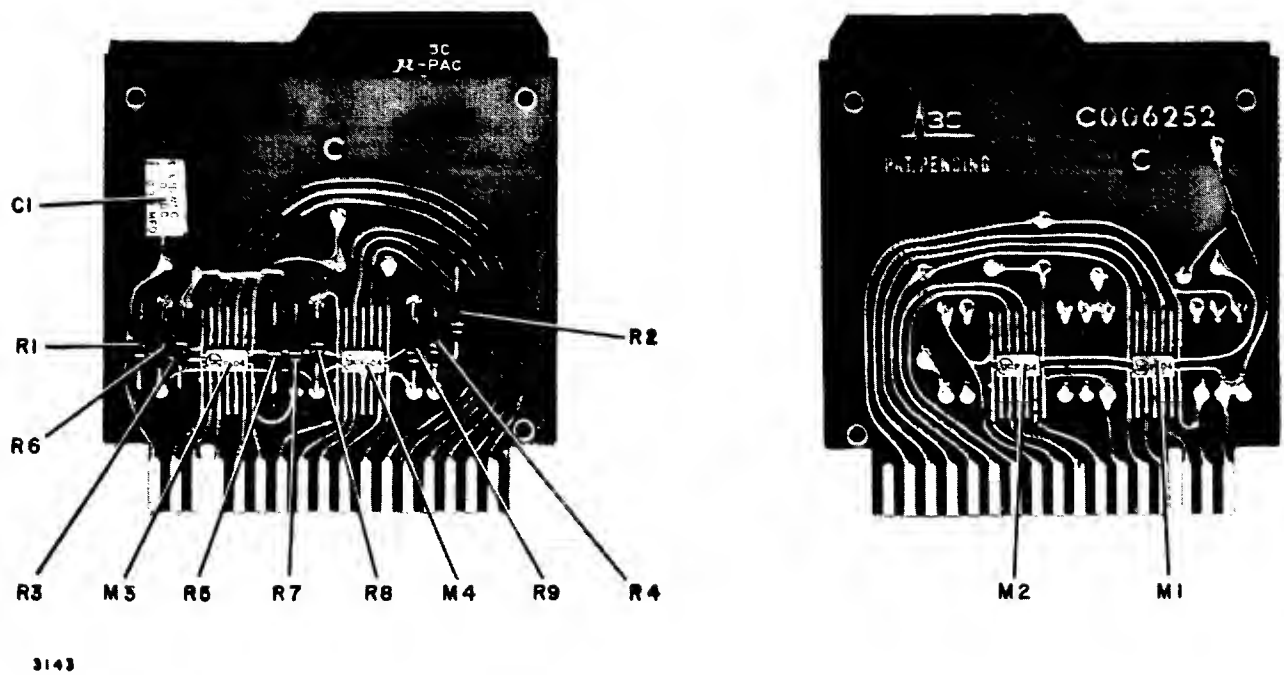


Figure A-50. Gated Flip-Flop PAC, Model CC-089,  
Schematic Diagram and Logic Symbol

## Parts Location



## Electrical Parts List

Ref. Desig.	Description	3C Part No.
M1-M4	MICROCIRCUIT: F-04, flip-flop integrated circuit	950 100 004
C1	CAPACITOR, FIXED, PLASTIC DIELECTRIC: 0.033 $\mu$ f $\pm$ 20%, 50 vdc	930 313 016
R1	RESISTOR, FIXED, COMPOSITION: 22K $\pm$ 5%, 1/4w	932 007 081
R2-R9	RESISTOR, FIXED, COMPOSITION: 51K $\pm$ 5%, 1/4w	932 007 090

Figure A-51. Gated Flip-Flop PAC, Model CC-089,  
Parts Location and Identification

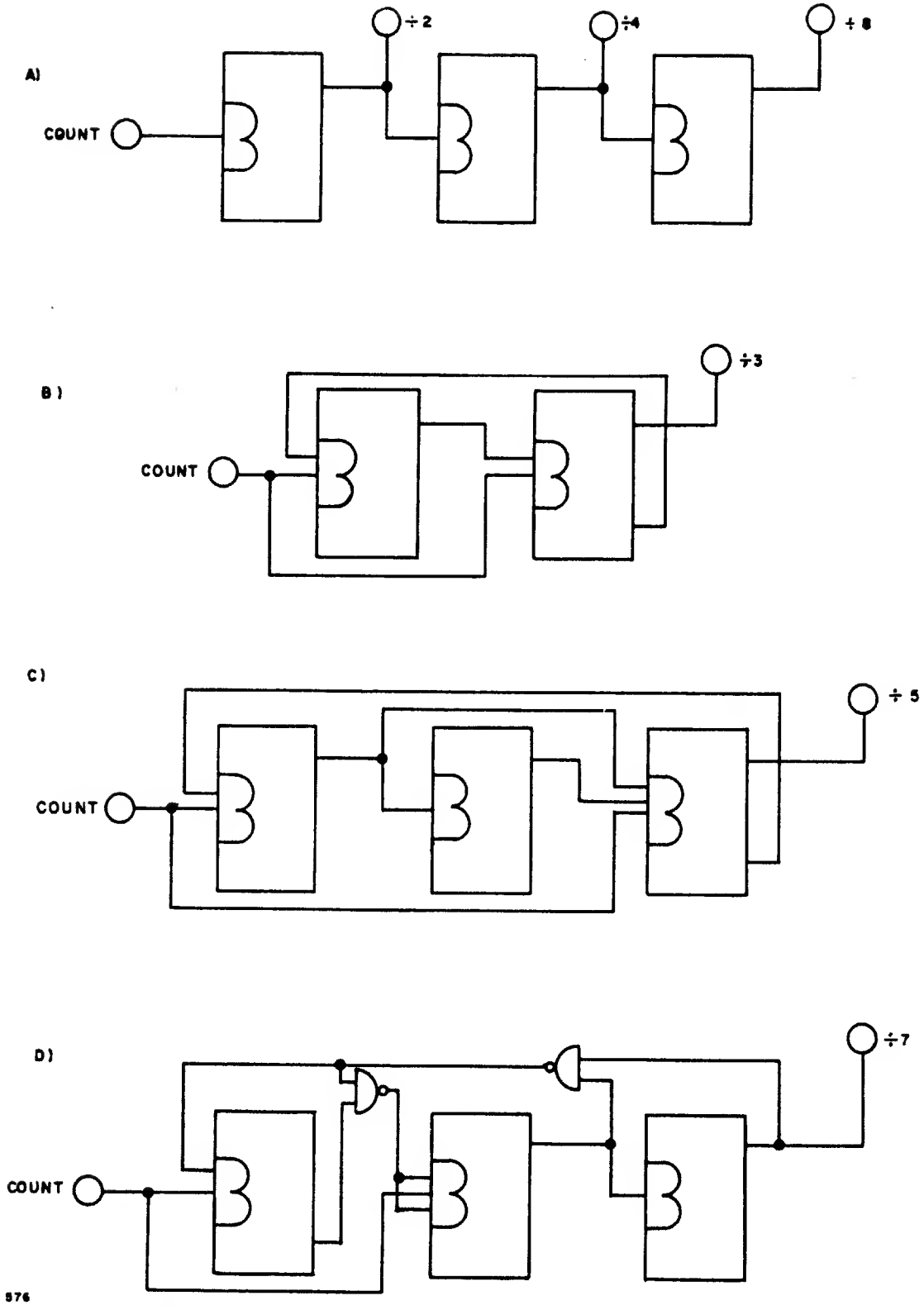
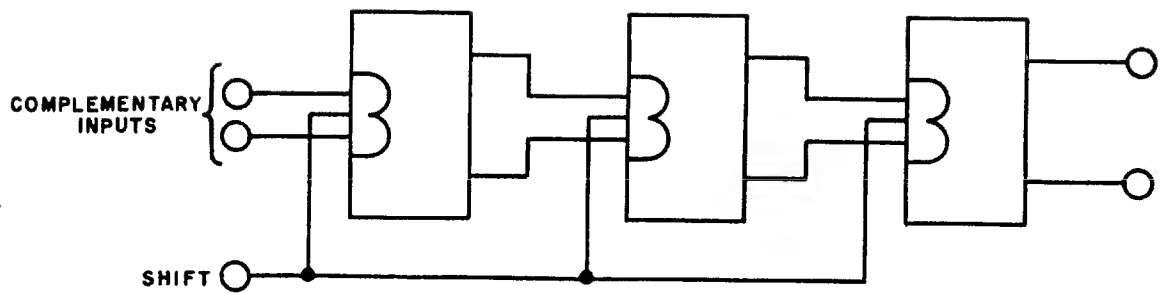
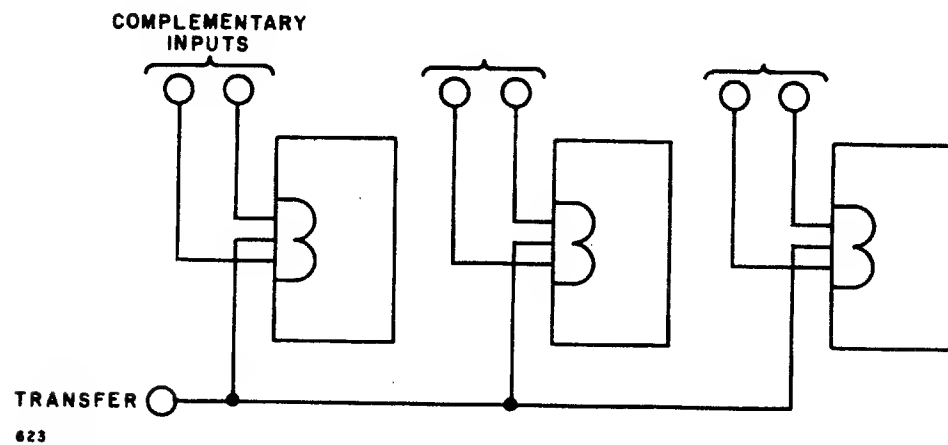


Figure A-52. Gated Flip-Flop PAC, Model CC-089, Counter Operation



623A

Figure A-53. Gated Flip-Flop PAC, Model CC-089,  
Shift Register Operation



623

Figure A-54. Gated Flip-Flop PAC, Model CC-089,  
Parallel Information Drop-In

## FAST CARRY COUNTER PAC, MODEL CC-091

The Fast Carry Counter PAC, Model CC-091 (Figures A-56 and A-57), contains eight pre-wired counter stages that can be set up by a few PAC connector jumpers to operate as an eight-stage binary counter or a two-digit BCD counter. In either configuration, carries are anticipated by gating structures, to reduce counter propagation delays.

Each stage has a dc set input for presetting a starting count, and a common reset input for clearing all eight stages simultaneously.

### INPUT AND OUTPUT SIGNALS

Count. -- The contents of the counter increase by one on the negative transition of the count input. This input is the same as the clock input of the integrated circuit flip-flop.

Common Reset. -- A signal at 0v for 80 nsec or longer on the common reset input clears all eight counter stages simultaneously.

BCD and BIN inputs. -- These points are to be connected as shown in Figure A-58 for binary counting or as shown in Figure A-59 for BCD counting.

### SPECIFICATIONS

#### Frequency of Operation (System)

DC to 5 mc

#### Input Loading

DC set inputs: 2/3 unit load each

Common reset: 5 unit loads

Complement: 2 unit loads

#### Output Drive Capability

<u>Output</u>	<u>Binary Mode</u>	<u>BCD Mode</u>
A and E	5 unit loads each	5 unit loads each
$\bar{A}$ and $\bar{E}$	8 unit loads each	8 unit loads each
B and F	5 unit loads each	6 unit loads each
$\bar{B}$ and $\bar{F}$	8 unit loads each	8 unit loads each
C and G	6 unit loads each	7 unit loads each
$\bar{C}$ and $\bar{G}$	8 unit loads each	8 unit loads each
D	6 unit loads each	6 unit loads each
H	8 unit loads each	8 unit loads each
$\bar{D}$ and $\bar{H}$	8 unit loads each	6 unit loads each

Circuit Delay

Counter propagation delay per group of 4 stages:	100 nsec (max)
Counter propagation delay for the 8 stage counter:	200 nsec (max)
DC set input to set output, or common reset input to reset output:	80 nsec (max)
DC set input to reset output, or common reset input to set output:	60 nsec (max)

Current Requirements

+6v: 200 ma (max)

Power Dissipation

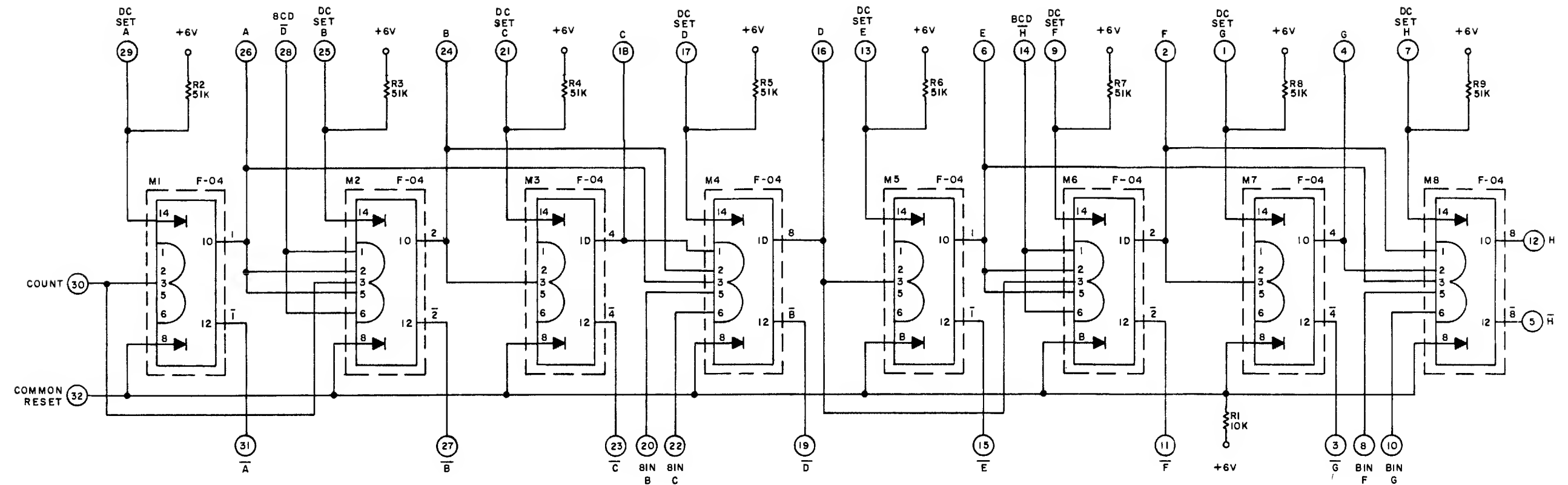
1.2w (max)

Handle Color Code

Blue

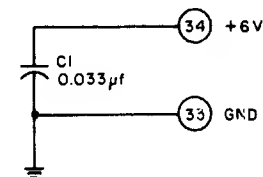
## APPLICATIONS

Figure 3 shows the  $\mu$ -PAC wired as an 8-bit binary counter. Frequency division by multiples of 2, up to 256, may be attained. Figure 4 shows the  $\mu$ -PAC wired as a 2-decimal digit BCD counter. The counter can be preset to a number by first resetting all stages, then setting only the appropriate ones.



# LEGEND

- (1) PIN NUMBER OF PAC
- 12 PIN NUMBER OF MICROCIRCUIT
- M3 REFERENCE DESIGNATION OF MICROCIRCUIT
- F-04 TYPE OF MICROCIRCUIT



## SCHEMATIC

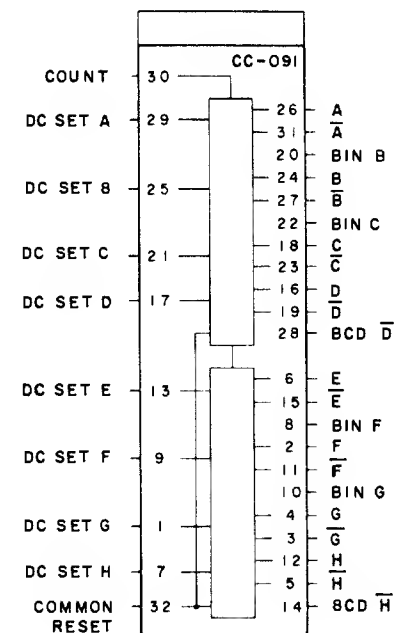
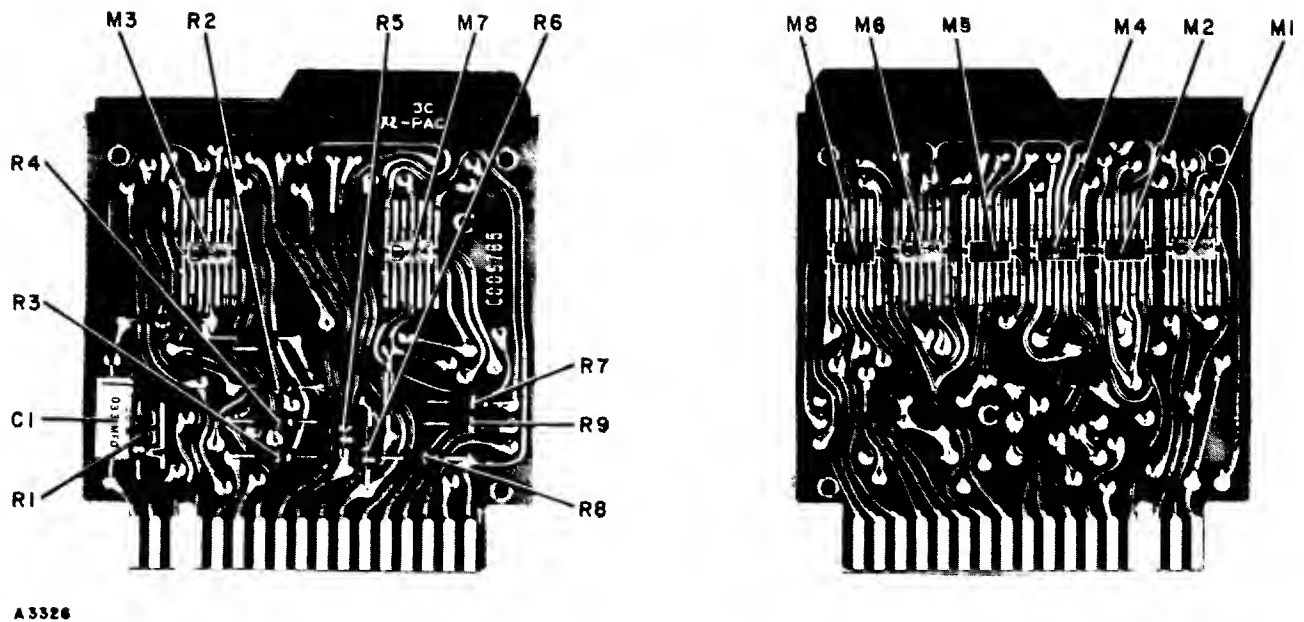


Figure A-56. Fast Carry Counter PAC, Model CC-091, Schematic Diagram and Logic Symbol



## Parts Location



## Electrical Parts List

Ref. Design.	Description	3C Part No.
M1-M8	MICROCIRCUIT: F-04, flip-flop integrated circuit	950 100 004
C1	CAPACITOR, FIXED, PLASTIC DIELECTRIC: 0.033 $\mu$ f $\pm$ 20%, 50 vdc	930 313 016
R1	RESISTOR, FIXED, COMPOSITION: 10 K $\pm$ 5%, 1/4w	932 007 073
R2-R9	RESISTOR, FIXED, COMPOSITION: 51 K $\pm$ 5%, 1/4w	932 007 090

Figure A-57. Fast Carry Counter PAC, Model CC-091,  
Parts Location and Identification

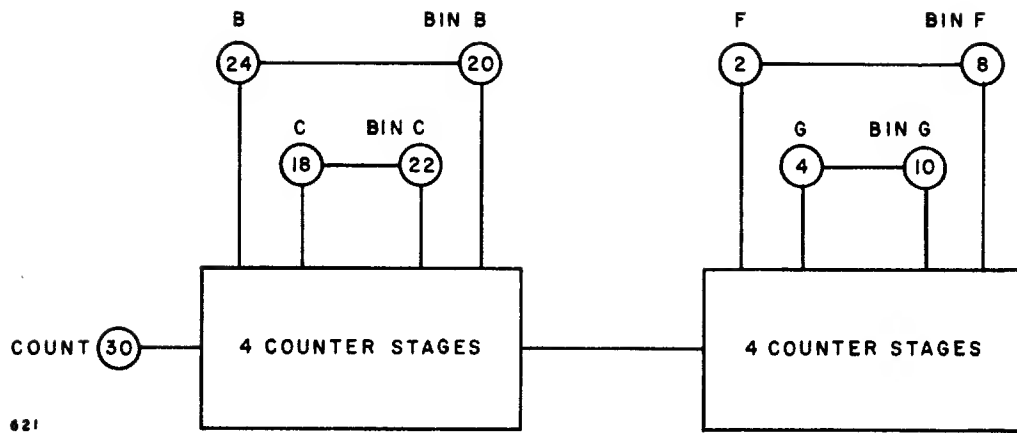


Figure A-58. Fast Carry Counter PAC, Model CC-091,  
Jumper Connections for Binary Counting

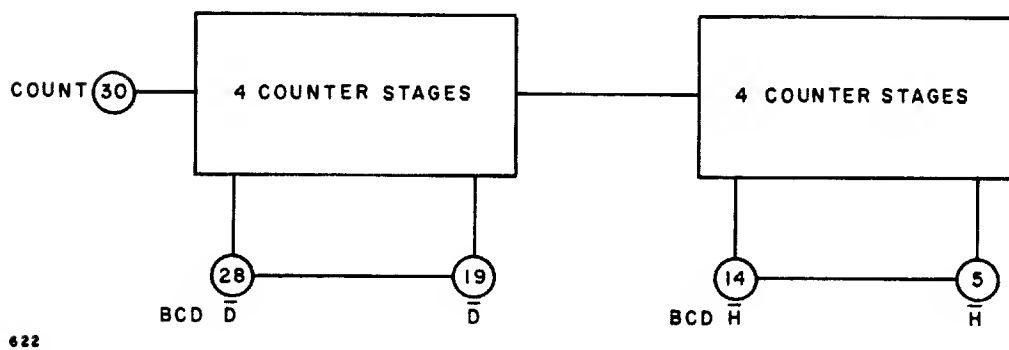


Figure A-59. Fast Carry Counter PAC, Model CC-091,  
Jumper Connections for BCD Counting

## DRIVER PAC, MODEL CC-480

The CC-480 Driver PAC, Model CC-480 (Figure 1), contains six dual four-input power NAND gates without collector pullup. An external resistor is added at different values for different output drive capability. Connect signal pins 2, 12, and 22 to a signal-ground pin other than pin 33 of this PAC.

SPECIFICATIONS ( $V_{cc} = 6$  volts)Input Loading

Pins 1, 4, 6, 7, 11, 13, 16, 18, 19, 21, 23, 29: 1.6 mA (max)

Pins 25, 26, 28, 30: 3.2 mA (max)

Pins 3, 8: 6.4 mA (max)

Output Loading

Pins 5, 9, 10, 14, 15, 17, 20, 24, 27, 31: 34 mA (max)

Pin 32: 64 mA (max)

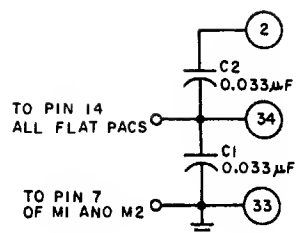
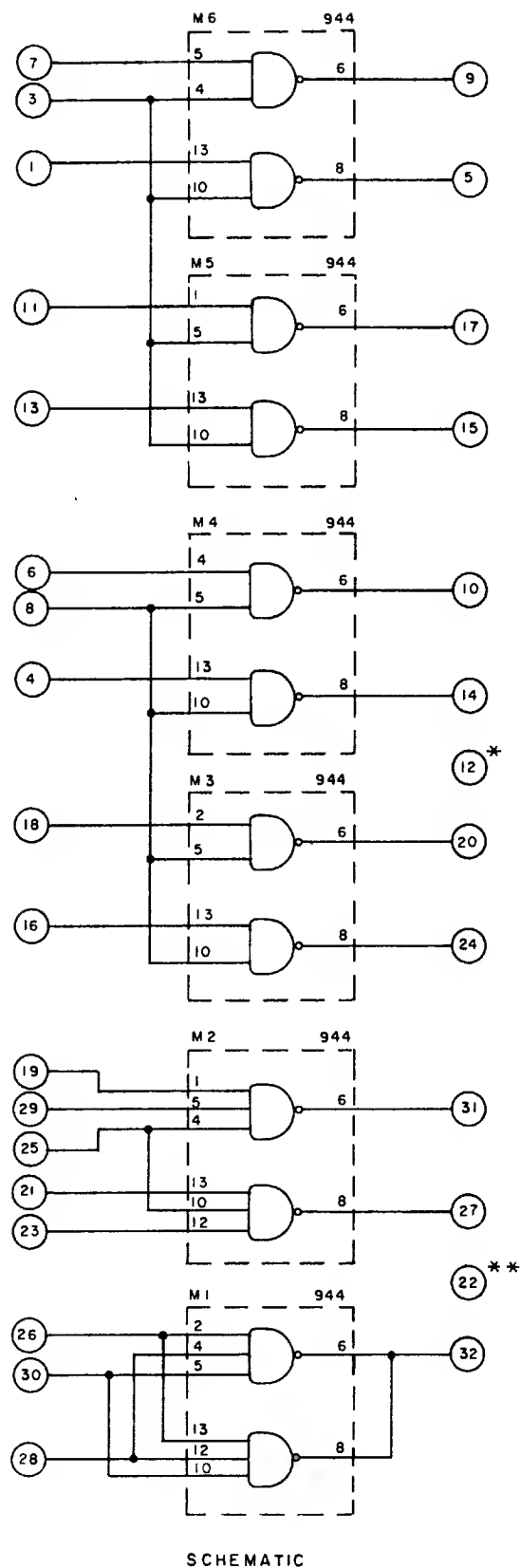
Typical Delay (two gates)

From input to pins 7, 11, 6, to output pins 5, 15, 14:  $Td_1$  and  $Td_2 = 105$  ns.

From input pin 26 to output pin 32:  $Td_1$  and  $Td_2 = 60$  ns.

## Electrical Parts List

Ref. Desig.	Description	Part No.
C1, C2	CAPACITOR, FIXED, PLASTIC: .033 $\mu$ F $\pm 20\%$ , 50 Vdc	70 930 313 016
M1 - M6	MICROCIRCUIT: 944, Dual Power NAND Gate	70 950 105 008



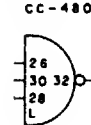
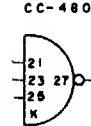
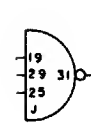
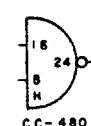
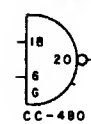
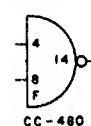
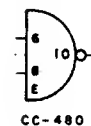
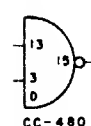
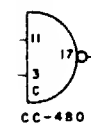
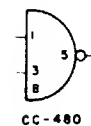
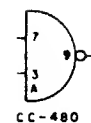
## LEGEND

- ① PIN NUMBER OF PAC
- ② PIN NUMBER OF MICROCIRCUIT
- M3 REFERENCE DESIGNATION OF MICROCIRCUIT
- 930 TYPE OF MICROCIRCUIT

## NOTE:

CONNECT SIGNAL PINS 2, 12, AND 22 TO A SIGNAL GROUND PIN OTHER THAN PIN NUMBER 33 OF THIS PAC.

- \* TO PIN 7 OF M5 AND M6
- \*\* TO PIN 7 OF M3 AND M4



## LOGIC SYMBOL

Figure 1. Driver PAC, Model CC-480  
Schematic Diagram and Logic Symbol

USERS' REMARKS FORM

TITLE:

DOC. PART NO. \_\_\_\_\_

DATED \_\_\_\_\_

ERRORS NOTED:

Fold

SUGGESTIONS FOR IMPROVEMENT:

Fold

DATE \_\_\_\_\_

FROM: NAME \_\_\_\_\_

COMPANY \_\_\_\_\_ M/S \_\_\_\_\_

TITLE \_\_\_\_\_

ADDRESS \_\_\_\_\_

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